-TR-94-75
Technical Report

ANALOG MICROCIRCUIT FAULT PREDICTION

Georgia Institute of Technology

Richard M. Ingle, John H. Bordelon, Michael J. Willis,
C. David Stokes

APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED.

Rome Laboratory
Air Force Materiel Command
Griffiss Air Force Base, New York

This report has been reviewed by the Rome Laboratory Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RL-TR-94-75 has been reviewed and is approved for publication.

APPROVED: E. Paul Ratazzi

E. PAUL RATAZZI
Project Engineer

FOR THE COMMANDER John J. Bart

JOHN J. BART, Chief Scientist
Reliability Sciences

If your address has changed or if you wish to be removed from the Rome Laboratory mailing list, or if the addressee is no longer employed by your organization, please notify RL (ERDA) Griffiss AFB NY 13441. This will assist us in maintaining a current mailing list.

Do not return copies of this report unless contractual obligations or notices on a specific document require that it be returned.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	April 1994	Final - -

4. TITLE AND SUBTITLE
ANALOG MICROCIRCUIT FAULT PREDICTION

5. FUNDING NUMBERS
C - F30602-88-D-0025,
PE - 62702F Task 0050
PR - 2338
TA - 01
WU - PJ

6. AUTHOR(S)
Richard M. Ingle, John H. Bordelon, Michael J. Willis,
C. David Stokes

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Georgia Tech Research Institute
Centennial Research Bldg
Georgia Institute of Technology
Atlanta GA 30332-0420

8. PERFORMING ORGANIZATION REPORT NUMBER
A-9285

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERDA)
525 Brooks Rd
Griffiss AFB NY 13441-4505

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
RL-TR-94-75

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: E. Paul Ratazzi/ERDA/(315) 330-2946

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)
This report documents an effort to determine the feasibility of constructing a realistic fault set for a given analog microcircuit from the information provided by a microcircuit yield simulator program. A methodology for this was developed and demonstrated using a simple PMOS process. The fault set which was generated demonstrates that it is possible to define how process defects affect electrical performance through the use of high level circuit models. The fault set can be ranked by probability of occurrence, and is suitable for use by a circuit simulation program.

14. SUBJECT TERMS
Analog, Microcircuit, Testability, Failure, Fault, Fault Modeling, Fault Simulation, Error, Testing

15. NUMBER OF PAGES
98

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	UL

Table of Contents

List of Figures

List of Tables

List of Acronyms and Abbreviations

ABCMOS	-- Advanced Bipolar CMOS, an Analog Devices, Inc., process
AC	-- alternating current
ASIC	-- Application Specific Integrated Circuit
cm-2	-- centimeters squared (reciprocal)
CMOS	-- Complementary Metal Oxide Semiconductor
DC	-- direct current
FABRICS	-- FABRication of Integrated Circuits Simulator
FASTRACK	-- (software product name, derivation unknown)
GT PMOS	-- Georgia Tech Positive Metal Oxide Semiconductor
GTRI	-- Georgia Tech Research Institute
IBM	-- International Business Machines
IC	-- integrated circuit
microns/min	-- microns per minute
MOS	-- Metal Oxide Semiconductor
MOSFET	-- Metal Oxide Semiconductor Field Effect Transistor
MOSIS	-- Metal Oxide Semiconductor Implementation System
NMOS	-- Negative Metal Oxide Semiconductor
PDFAB	-- (software product name, derivation unknown)
PEW	-- Process Engineer's Workbench
PISCES	-- (software product name, derivation unknown)
PMOS	-- Positive Metal Oxide Semiconductor
PMOSFET	-- Positive Metal Oxide Semiconductor Field Effect Semiconductor
PREDITOR	-- Process Editor
PROD	-- (software product name, derivation unknown)
PSPICE	-- (software product name, version of SPICE made by MicroSim, Inc.)
RYE	-- Realistic Yield Evaluator
SPICE	-- Simulation Program With Integrated Circuit Emphasis
SPICE2	-- (advanced version of SPICE)
SPICES	-- (software product name, derivation unknown)
SUPREM	-- (software product name, derivation unknown)
UCLA	-- University of California, Los Angeles
VLSI	--Very Large Scale Integration

Analog Microcircuit Fault Prediction

Section I
Introduction

1.1 Objective

The objective of this program is to develop techniques for predicting faults in analog microelectronic devices using yield simulators.

1.2 Scope

This report documents an effort to determine the feasibility of and procedures necessary for constructing a fault set for a given analog microcircuit from the information provided by a microcircuit yield simulator program (such as Carnegie-Mellon's FABRICS). The resulting fault set defines how the defects affect the electrical performance of the microcircuit, and are ordered by the probability of occurrence. The fault set contains all the necessary information such that a circuit simulator file, representing the microcircuit's faulted state, can be generated. Only singly-inserted failures are considered.

1.3 Executive Summary

Although the objective of the program was originally to develop techniques for predicting faults in analog microelectronic devices using yield simulators, a literature search revealed that integrated circuit process simulators are more appropriate than yield simulators for analog microcircuit fault prediction. Yield simulators (and associated fault simulators) tend to focus on digital circuit performance. As a result, these simulators often assume only the existence of shorts, opens, or "stuck at" faults. Analog circuit analysis requires that the process variations that occur in the fabrication of analog microcircuits be accounted for in the determination of SPICE2 circuit parameters. The SPICE2 circuit parameters are then used in a SPICE circuit simulator to determine the actual performance parameters of a benchmark microcircuit. The literature search also resulted in the choice of a program called PREDITOR (PRocess EDITOR) as the process simulator.

One goal of the program was to select a commercial analog microcircuit process for simulation by the process simulator. GTRI discussed this goal with several analog microcircuit vendors. With one exception, the vendors treat the fabrication processes as highly proprietary. While recognizing the need for this research area, the companies generally are unwilling to release process information to outside organizations. However, Analog Devices, Incorporated, provided GTRI with detailed data regarding their proprietary ABCMOS (Advanced Bipolar CMOS) process. After examining the data, GTRI determined that the process is too complex to attempt to simulate, given the resources available for this effort.

As an alternative to a complex commercial process, the Georgia Tech Microelectronics Research Center has developed a simple PMOS process that is used in student fabrication classes. Because of the simplicity of this process, it was selected for simulation by PREDITOR.

A quantity of statistical data on MOSIS (Metal Oxide Semiconductor Implementation System) SPICE2 circuit parameters was available, and was used to study the effect of SPICE2 device parameters on benchmark circuit performance parameters. However, the MOSIS process data itself was not available, since MOSIS processes are considered proprietary. MOSIS is a consortium serving MOS IC fabrication needs of universities and industry.

The principal result of this project is a methodology for converting process simulator inputs to circuit models for the purpose of generating likely fault models for a given microcircuit fabricated in a given process. When these process simulator inputs represent failures, the resulting circuit models are fault models of these failures. The methodology that was developed is illustrated using a differential amplifier as a benchmark microcircuit. Process parameters were used as input to the process simulator, which then produced SPICE2 device parameters. These device parameters were then used by a circuit simulation program, PSPICE, to measure carefully chosen circuit performance parameters for the benchmark differential amplifier circuit. This process was repeated several times with the values of the individual process parameters increased, one at at time, by **10%** (in the methodology this is a two standard deviation change). The resulting changes in the circuit performance parameters show which process parameters have the greatest influence on circuit performance.

Section II
Literature Search

2.1 Significant Articles

The Analog Microcircuit Fault Prediction research effort began with an investigative literature search. The purpose of the search was to gather information on current methods of yield simulation and defect prediction that would lead to the selection of a defect simulation method. General search topics included: yield simulation, fault prediction, and process simulation. Emphasis was placed on the applicability of simulation methods to analog circuitry. In addition to literature resources, experts from Georgia Tech and other institutions were consulted.

2.2 Results

The majority of relevant publications came from Carnegie-Mellon University, where research in process and yield simulators and simulation is currently underway. Outside of Carnegie-Mellon, research publications were identified which discuss general IC failure and yield research, digital IC yield improvement, and mathematical algorithm justifications.

Relevant research publications from sources other than Carnegie-Mellon include papers by researchers from IBM, University of Illinois, UCLA, University of Maryland, and Beijing University. Dr. Charles H. Stapper (IBM) had investigated general causes of IC failure and spatial fault simulation [17, 26, 28]. At the University of Illinois, yield maximization algorithms were studied [25]. At the University of California at Los Angeles, digital IC yield improvement was examined [21, 22]. Mathematical algorithm justifications for yield statistics and analog fault diagnosis were researched at the University of Maryland [23], IBM [29], and Beijing University [35].

Several Carnegie-Mellon articles described simulators and simulation methods for analyzing IC manufacturing failures and their effect on production yield. Early research involved the development of a methodology for modeling random fluctuations of the IC manufacturing process [24]. A later simulator (PROD [12]) was developed to identify the variations in process conditions that cause drops in yield. The diagnosis of parametric faults occurring in the IC manufacturing process was also examined [14]. An analytically-based tool named RYE [44] (Realistic Yield Evaluator) was created to determine the probability of structural failures for VLSI circuits. All of these simulation methodologies involved the use of statistical simulations employing the statistical process simulator named FABRICS [30].

FABRICS (FABRication of Integrated Circuits Simulator) was designed to provide a faster simulation by employing analytical models as solutions to the partial differential equations that govern the fabrication process. Although restricted or simplified conditions were applied in order to facilitate the use of these simpler models, the simulations were found to yield reasonable results. FABRICS accepts process parameters, integrated circuit layout, and process disturbances as input and generates device model parameters. This tool became the engine for more advanced process simulators.

Two workstation-based tools for modeling the VLSI fabrication process were more recently developed with FABRICS at the heart of their design. The first simulator, called PEW [45] (Process Engineer's Workbench), provided a graphical interface to a collection of tools integrated together into one package. In addition to the statistical simulation capabilities of FABRICS, PEW added incremental process simulation, a means for evaluating the I-V or C-V characteristics for basic devices, and the ability to facilitate smooth transitions between process parameters and circuit simulation.

A second software package, called PREDITOR [47, 48, 51] (PRocess EDITOR), is essentially a refinement of previous process editing and statistical simulation tools, combining features of both PEW and FABRICS. PREDITOR incorporates a new flexible database format for storing and retrieving process and device simulation information. Other changes include improvements in the graphical interface. PREDITOR was made available to GTRI for this research by Carnegie-Mellon. A commercial version of PREDITOR, called PDFAB, is also available. It was hoped that PDFAB might have corrected some of the problems that were encountered with PREDITOR, as mentioned later in this report. A copy of PDFAB was sought for this research but was not obtained before the conclusion of the research.

Fault and yield simulators for digital microcircuits generally assume that faults are restricted to improper state operation. This occurs when outputs are stuck at a logic low or high condition, or when outputs fail to respond correctly to defined digital input conditions. The digital fault and yield simulators further assume, in many cases, that electrical failures are due to catastrophic spot defects on the chip. These assumptions are not adequate for the determination of faults in analog microcircuits. For analog circuits, shifts in process parameters, as opposed to catastrophic defects, can cause significant shifts in device model parameters. These changes in device parameters cause variations in the electrical performance of the overall microcircuit. Thus, to investigate analog microcircuit faults, a process simulator that predicts the SPICE2 electrical parameters for the devices on a chip is the appropriate tool for investigation.

As a result of the literature search, software to facilitate fault simulation was evaluated on the basis of several criteria. The utility and versatility of the package were of great importance. A program that could accurately predict circuit faults to a statistically acceptable level for real-world processes was necessary. The availability of such a simulation tool in the public domain or at nominal cost was also required. In addition to purchase price, the costs in terms of hardware requirements and execution time should be kept to a minimum. A software package that would operate on popular UNIX workstation platforms requiring nominal memory and hard disk space was desired. Also, current simulator support and planned improvements would enhance the utility of the tool.

Several software packages developed outside Carnegie-Mellon University were considered. Among these, two simulation packages currently in use include FASTRACK and SUPREM with PISCES or SPICES.

FASTRACK was developed by Harris Semiconductor for customer use in developing Harris based Application-Specific Integrated Circuits (ASIC's). It performs schematic capture, yield analysis, IC layout, and SPICE simulation for Harris

Semiconductor processes. One advantage of this system is the fact that the simulator has already been tuned to the processes it simulates. Unfortunately, these processes are limited to those used by Harris in their fabrication. Another disadvantage of the system was the high cost, which was on the order of $90,000.

SUPREM and PISCES were developed as a process-device simulation combination. SUPREM is a two-dimensional process simulator that uses physically based models to produce very accurate results. Models of the fabrication steps described by partial differential equations are solved using numerical techniques. Unfortunately, this added complexity leads to time-intensive simulations that make statistical simulations difficult to perform. For this reason, software developers have not included many statistical tools with packages containing these tools. PISCES is a two-dimensional device simulator that uses SUPREM output to determine the electrical behavior and properties of specific device structures. Another equivalent device simulator is called SPICES. It is an extension of PISCES that allows simple circuit elements to be included in the PISCES model simulation.

PREDITOR was chosen for this research after consideration of the factors mentioned above. Those factors principally responsible for its selection were its currency, capability for parametric analysis, computer platform compatibility, its ability to analyze both bipolar and MOS processes, and its cost.

2.3 Description of Process Simulator

The choice of a process simulator for this research is of primary importance. The process simulator was a principal tool used to provide information on the way in which IC process variations affect circuit performance parameters. Two readily available software packages, PREDITOR and PSPICE, were the principal tools used to implement the methodology. PSPICE is a standard and highly regarded circuit simulator which works with either active device equivalent circuit parameters or device physical dimensions and device parameters produced by a process simulator. PREDITOR is a process simulator that produces device parameters from a process description. The process description consists of a process flow file and mask artwork files. Since PSPICE is a well known software package, the following description will be limited to PREDITOR.

PREDITOR requires as input a process flow file, which is a detailed list of process steps together with all process parameters, such as times, temperatures, dopant types and concentrations, and various other information. Statistics of these process parameters, expressed in mean and standard deviation, may also be supplied. PREDITOR uses these to determine statistics for the output information it produces. It is also necessary to provide, in the process flow file, in-line statements to specify measurements to be made on the various layers, if such measurements are desired. The process flow file is input using a form provided in the program. Mask artwork files must be provided in CIF format, but can be modified or generated in PREDITOR.

PREDITOR outputs consist of text and graphical outputs. Active devices are automatically located, and their location displayed graphically. SPICE2 device parameters are supplied as text files for each device, provided that the appropriate in-

line measurements have been specified in the process flow file. I-V curves are also displayed for each device. Cross section cuts of any device can be specified and then calculated and displayed. E-field plots and carrier concentrations can also be displayed. If a point is specified on the chip, dopant concentration curves as a function of depth will be produced. However, information can also be generated after the completion of any number of the specified process steps, to show the progressive fabrication of device structures. In-line measurements can also be made. Statistics of most output parameters are also available. If desired, any one process parameter can be swept over a range and the effect on output parameters will be displayed. A sensitivity analysis of all output parameters as a function of input parameters may also be calculated.

Section III
Methodology

3.1 Background

The purpose of the methodology is to show, quantitatively, how process failures may be used to predict circuit faults. To this end, the methodology is primarily a sensitivity analysis, where one process parameter is incremented at a time, by two standard deviations, and the performance parameters are then determined by simulation for each case. The process variations are used as input to PREDITOR, which produces SPICE2 device parameters. The resulting device parameters are incorporated into an input file in PSPICE, which then determines the microcircuit performance parameters by simulation.

A multiple path approach to demonstrating the methodology was taken. This approach is illustrated in Figure 1 below. This multiple path approach was taken because of the difficulty of fully implementing the process with any one path. SIS process parameters, being proprietary, are not available, and so cannot be ed into PREDITOR. GT PMOS process parameters are available, and test data is available, so this process allows the complete end-to-end methodology to be carried out. The ABCMOS process is far too complex to be input into PREDITOR within the scope of the current research project. It was found, even with the relatively simple GT PMOS process, that the values for the process parameters had to be extensively adjusted for PREDITOR to yield SPICE2 device parameters that corresponded to working MOS devices. Without the benefit of additional experience, this tuning would be difficult with the complex ABCMOS process.

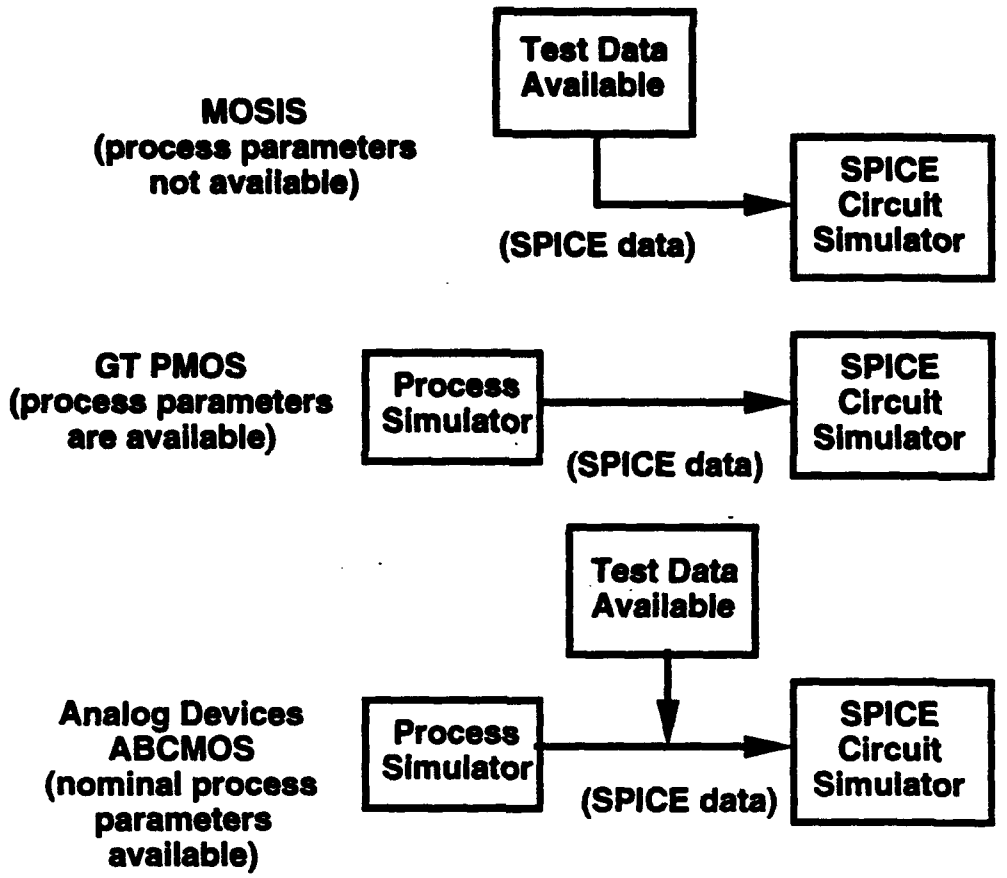

Figure 1. Parallel Tasks

3.2 MOSIS Device Data

Process parameters are not available for MOSIS devices, because the processes used by MOSIS are considered proprietary. However, test data is available and in sufficient quantity that statistics for device SPICE parameters can be calculated. Appendix A shows device parameters and statistics for NMOS and PMOS devices with lengths of 2 and 10 microns. The importance of this statistical data is that it allows verification of the SPICE simulator as an important tool in the overall methodology chain. These statistics are used to develop a limited background on SPICE parametric effects on circuit performance. The resulting circuit performance parameters may also be expressed in a statistical fashion.

3.3 Georgia Tech PMOS Process

The Georgia Tech Microelectronics Research Center has developed a simple PMOS process that is used by students studying integrated circuit fabrication techniques in classes offered by the School of Electrical Engineering. The process flow is described in quantitative step-by-step detail in Appendix B. A qualitative description follows. This process is a simple one, and therefore well suited to this

initial research. Unfortunately, good statistics on this process are not available, because the devices fabricated by engineering students exhibit wide statistical variations in performance. The process starts with phosphorus doped silicon substrates. A dry oxidation step, followed by a wet oxidation step and another dry oxidation step, produces a field oxide over the substrate. A photolithography and etching step then defines the area for the source and drain diffusions. Boron is then deposited on the surface of the source and drain area and diffused into the substrate by elevating the temperature of the substrate; additional diffusion occurs during later process steps as the substrate is heated for other processes, such as during growth of gate oxide. A photolithography step is next used to allow the field oxide over the gate region to be etched away. A thinner oxide is then grown over the gate region using a dry oxidation step. A photolithography and etch step then opens holes through the gate oxide, which at this point covers the entire wafer, to allow for contacts to the source and drain regions. Aluminum is then evaporated onto the entire surface of the wafer and photolithographically etched to define the source, drain, and gate contacts.

Data was collected from a number of GT PMOS devices. Table 1 below shows the device parameters measured in the lab.

Table 1. GT PMOS Device Parameters

W/L	lambda	VTO	Kp	gamma
200/200	6.84e-03	1.98 V	7.80e-06 A/V^2	0.507
200/100	3.22e-03	1.99 V	8.00e-06 A/V^2	0.519
200/50	2.53e-03	1.97 V	8.12e-06 A/V^2	0.532
200/20	1.6e-02	1.95 V	8.90e-06 A/V^2	0.568
200/10	5.54e-02	1.89 V	1.15e-05 A/V^2	0.600

3.4 Analog Devices, Inc. ABCMOS Process

This was the only commercial microcircuit process that was made available for this research, but it is a state-of-the-art commercial process, producing both bipolar and CMOS devices. Analog Devices was both willing and cooperative in supplying this data, reflecting the fact that they consider this research to be very valuable to them. This is a very complex process, at least an order of magnitude more complex than the GT PMOS process. The difficulties experienced in getting PREDITOR to work with the GT PMOS process are greatly multiplied when the ABCMOS process is used in PREDITOR. As a result, using the ABCMOS process in PREDITOR was not within the scope of the present research.

3.5 Background Summary

The MOSIS path was successfully used to show the effects of SPICE parametric variation on benchmark circuit performance. The GT PMOS path was successfully used to show that PREDITOR may be used to generate SPICE device parameters from a process description and that the calculated parameters correspond to measured parameters. The ABCMOS path was not successful during the present effort, primarily due to the difficulty of characterizing the process in PREDITOR. It is hoped that

additional work with PREDITOR or PDFAB can produce a successful result at some future time.

3.6 MOSIS Path

The importance of investigating the MOSIS path is that a key element in the methodology is the effect that SPICE parameters have on circuit performance. The equation relating SPICE parameters to drain current is

$$I_D = (KW/2L)(V_{GS} - V_T)2(1 + \lambda V_{DS}),$$

$$\text{where } V_T = V_{TO} + \gamma\{(\varphi - V_{BS})^{1/2} - \varphi^{1/2}\}.$$

K = transconductance parameter.
W = width of MOS device channel.
L = length of MOS device channel.
λ = channel length modulation parameter
φ = strong inversion surface potential.
γ = bulk threshold parameter.
V_{GS} = gate to source voltage.
V_{DS} = drain to source voltage.
V_{BS} = bulk to source voltage
V_T = threshold voltage.
V_{TO} = threshold voltage for $V_{BS} = 0$.

It is important to demonstrate, using SPICE, that the selected SPICE device parameters (γ, V_{TO}, K, and λ) affect the electrical measurements that are chosen as benchmarks.

In order to correlate process failures to circuit faults, some particular microcircuit must be examined. SPICE2 device parameters produced by a process simulator, in this case PREDITOR, must be applied to the devices in the benchmark microcircuit and then the performance of this circuit must be calculated.

The differential amplifier is a common design element in analog integrated circuits. The differential inputs and outputs facilitate the use of feedback and cascading. When multiple differential amplifiers are cascaded for higher gain, they may be designed for matching input and output offsets. The performance of the differential amplifier is readily characterized in software and is easy to understand intuitively as well. Therefore, a MOSFET differential amplifier circuit has been chosen for use as the benchmark microcircuit in this research effort. The circuit used for the MOSIS device data is shown in Figure 2 below.

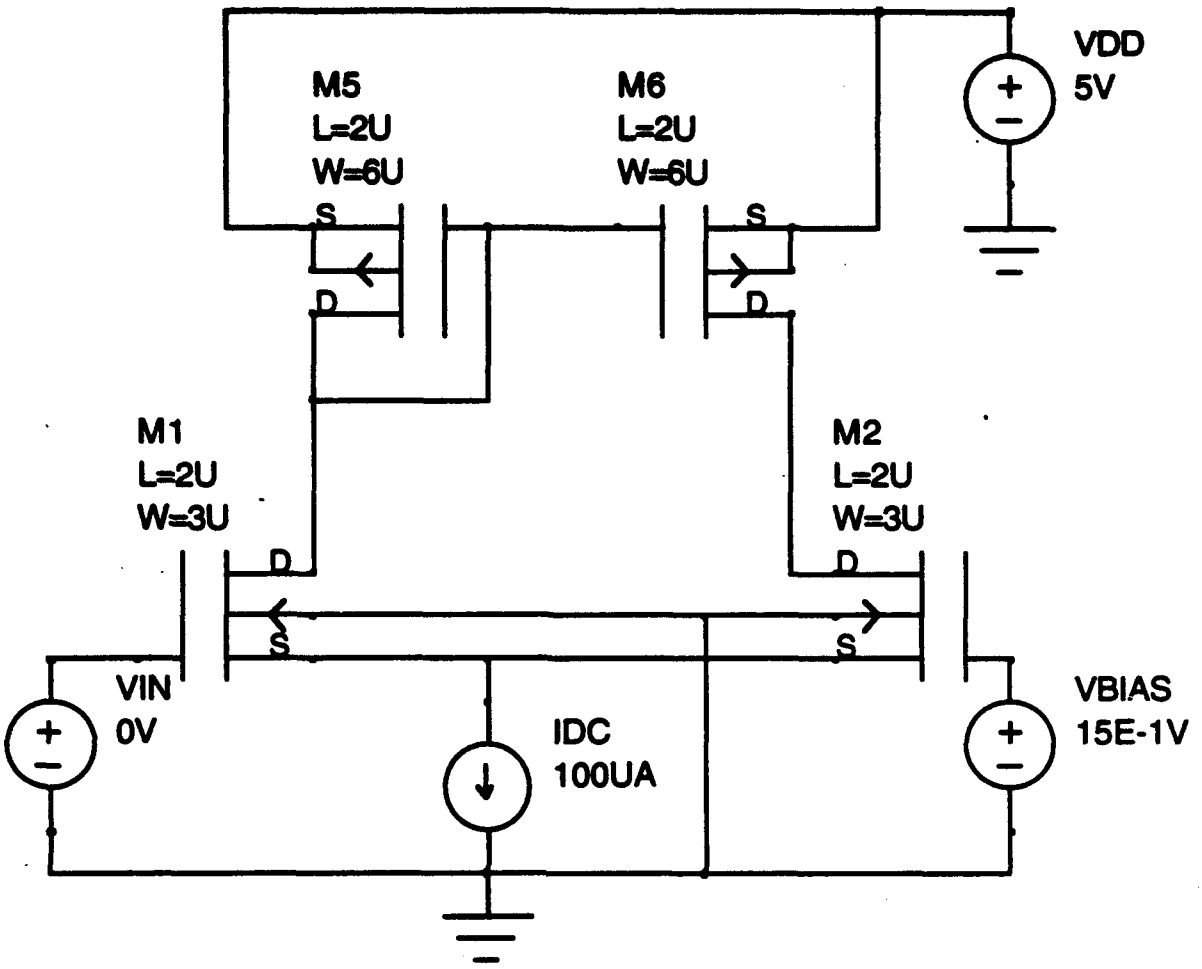

Figure 2. Benchmark Circuit Used For MOSIS Device Data

Many different DC and AC circuit performance measures can be considered for correlation to process failures. A given performance measure must have the appropriate SPICE2 model parameters available for simulation. PREDITOR can predict all of the SPICE2 parameters for a given device. However, it is cumbersome to verify all of the parameters in the laboratory. Those parameters which affect AC circuit performance are the most difficult to verify. As a result those parameters which affect DC circuit performance were selected. PREDITOR cannot predict the variation in process parameters that is a function of position on the chip. These variations result in device mismatches. Thus, performance parameters such as common-mode rejection ratio and offset voltages and currents cannot be utilized because they cannot be predicted.

Two performance parameters were chosen. They were large-signal voltage gain and large-signal transconductance, also referred to as DC voltage gain and DC transconductance. These parameters are functions of K, V_{TO}, λ, and γ, the principal SPICE2 parameters which are predicted by PREDITOR and measured. DC current drain was considered as a performance parameter but was rejected because an ideal

current source dominates the operation of the MOSIS circuit.

The results for the MOSIS path follow in a series of graphs of circuit performance, Figures 3 through 12. Results are shown for devices having length L = 2 μm and devices having length L = 10 μm. For each length, results for five different combinations of widths for the PMOS and NMOS devices are shown. Each graph is composed of a group of plots that are a result of a Monte Carlo simulation run in which the SPICE2 device parameters are allowed to vary over a range given by the parameter statistics. The SPICE parameter statistics for the MOSIS process are shown in Appendix A. The spread of these plots is an indication of the total variation in circuit performance resulting from all the variations in the individual device parameters.

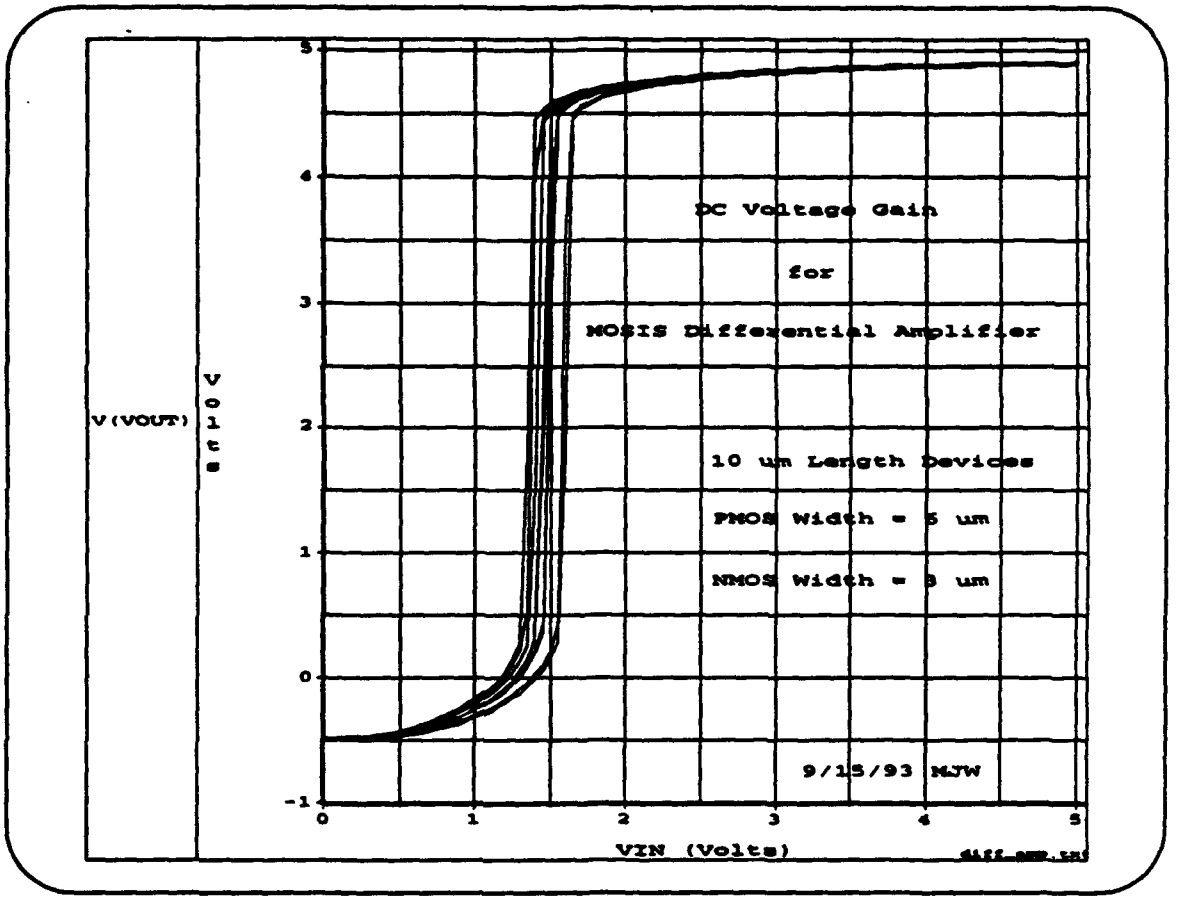

Figure 3. DC Voltage Gain For MOSIS Differential Amplifier L = 10 μm, W(PMOS) = 6 μm, W(NMOS) = 3 μm

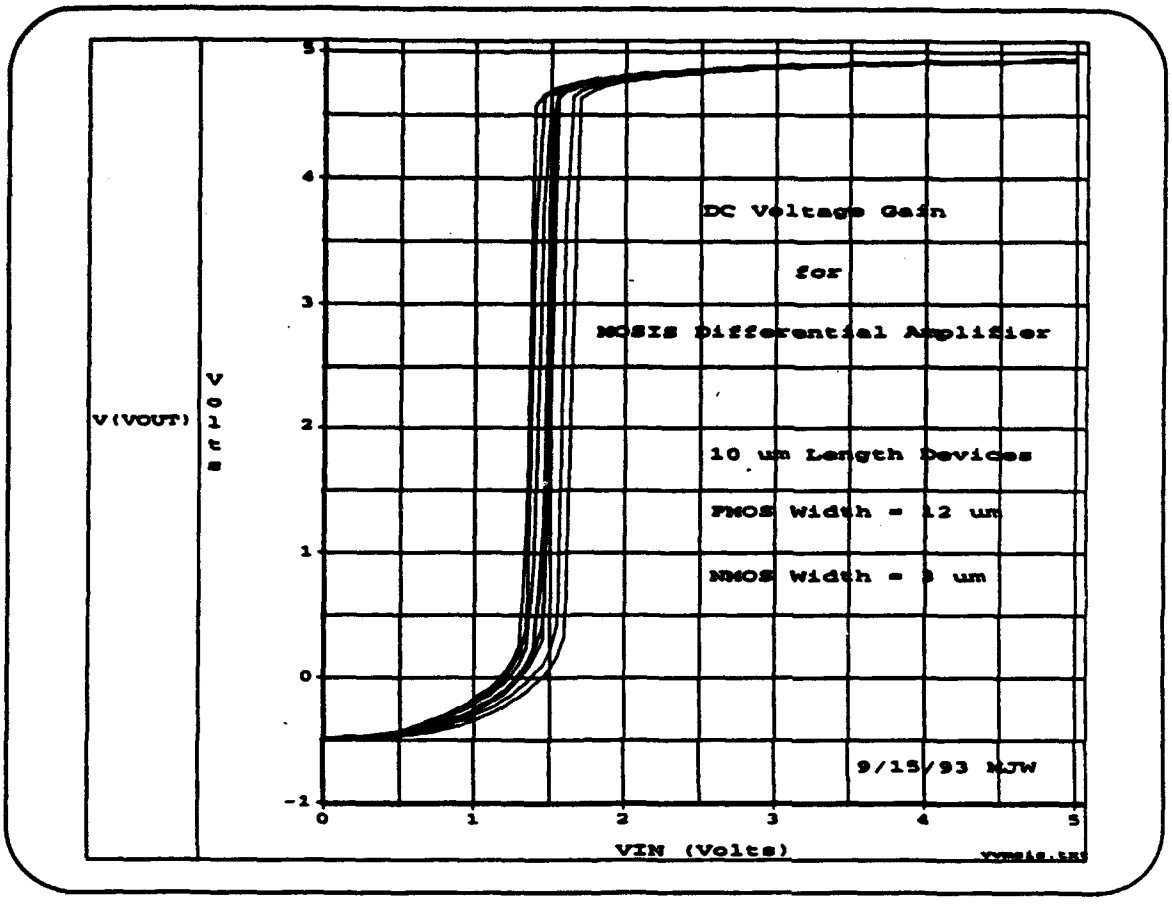

Figure 4. DC Voltage Gain For MOSIS Differential Amplifier L = 10 μm, W(PMOS) = 12 μm, W(NMOS) = 3 μm

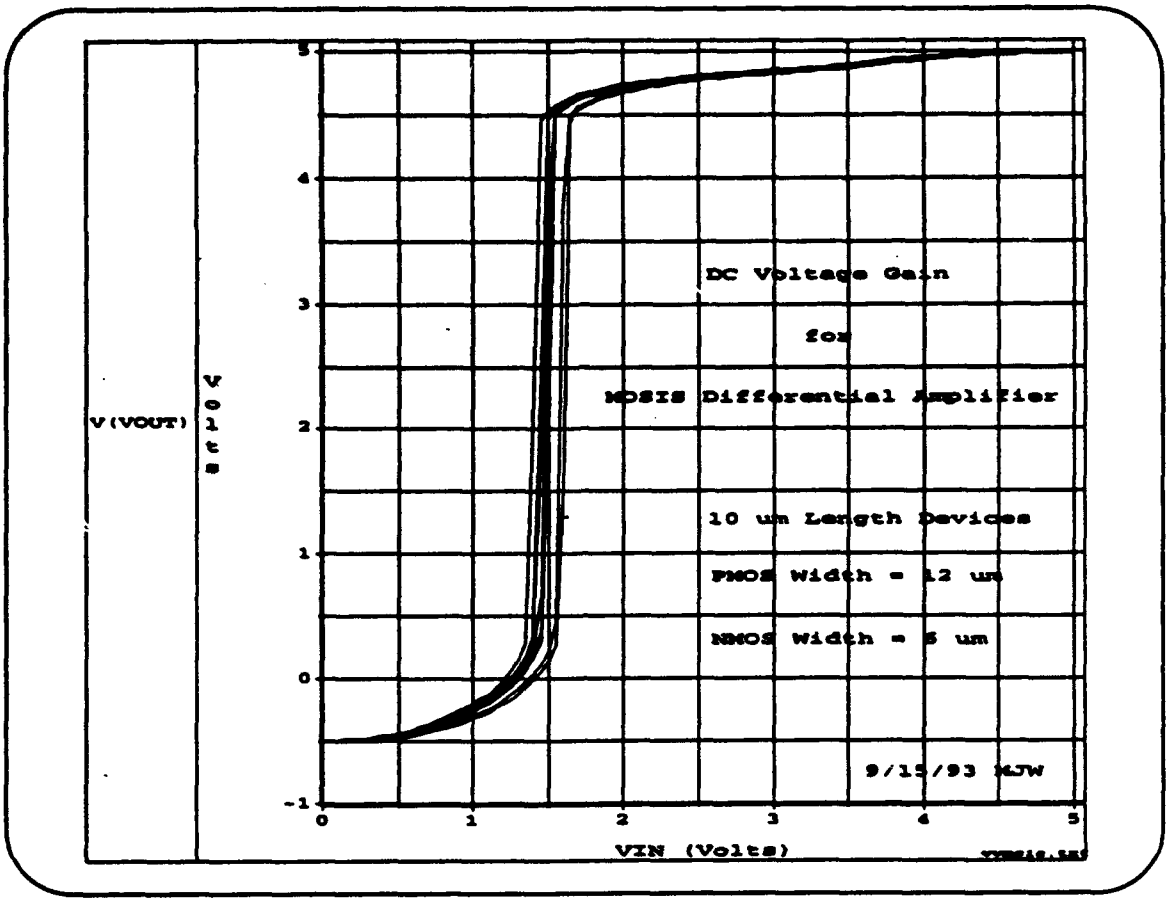

Figure 5. DC Voltage Gain For MOSIS Differential Amplifier L = 10 μm, W(PMOS) = 12 μm, W(NMOS) = 6 μm

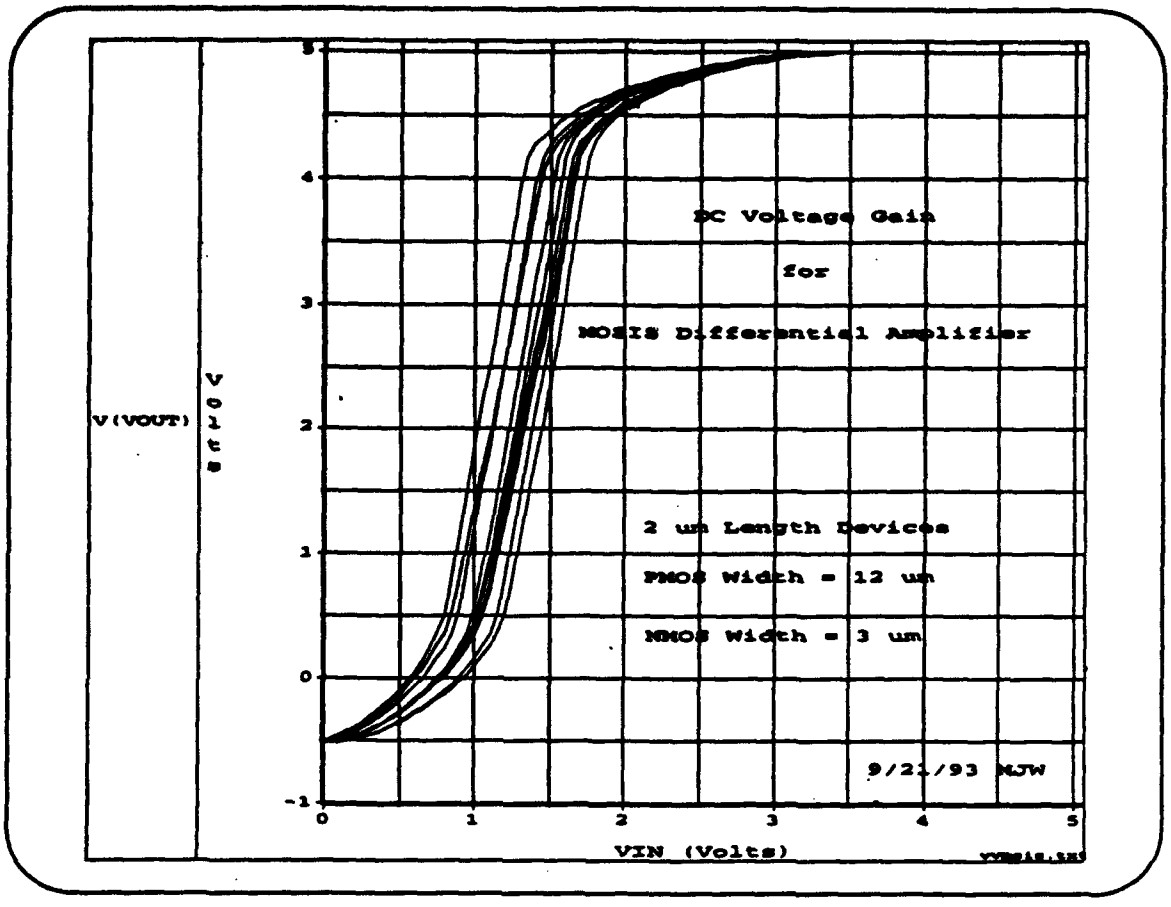

Figure 6. DC Voltage Gain For MOSIS Differential Amplifier L = 2 μm, W(PMOS) = 12 μm, W(NMOS) = 3 μm

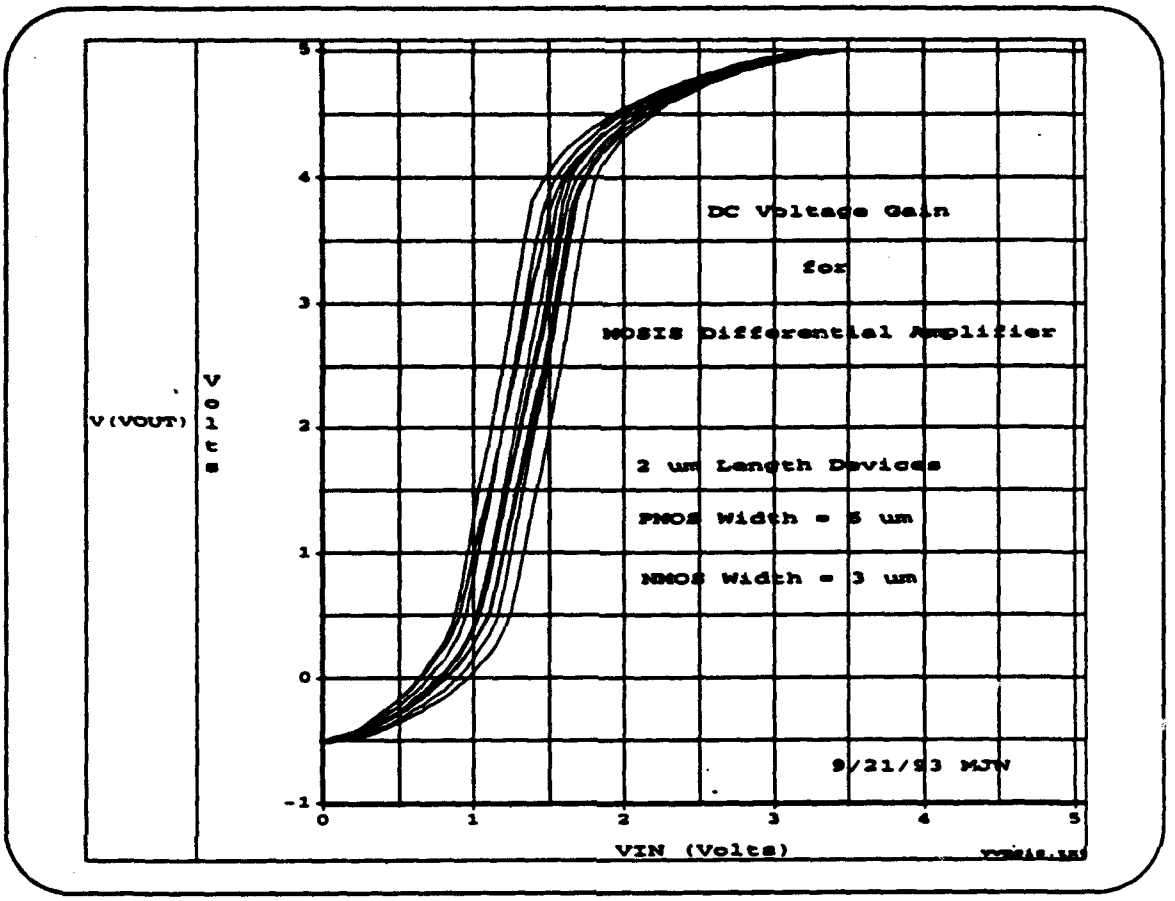

Figure 7. DC Voltage Gain For MOSIS Differential Amplifier L = 2 μm, W(PMOS) = 6 μm, W(NMOS) = 3 μm

The DC voltage gain plots above, Figures 3 through 7, show that the process variations experienced in the MOSIS process and reflected in the device parameters do not significantly affect voltage gain. The principal effect is that of an output offset. The device parameter statistics that were used were gathered over time and across many wafers. Device parameter statistics might be expected to be tighter across an individual wafer.

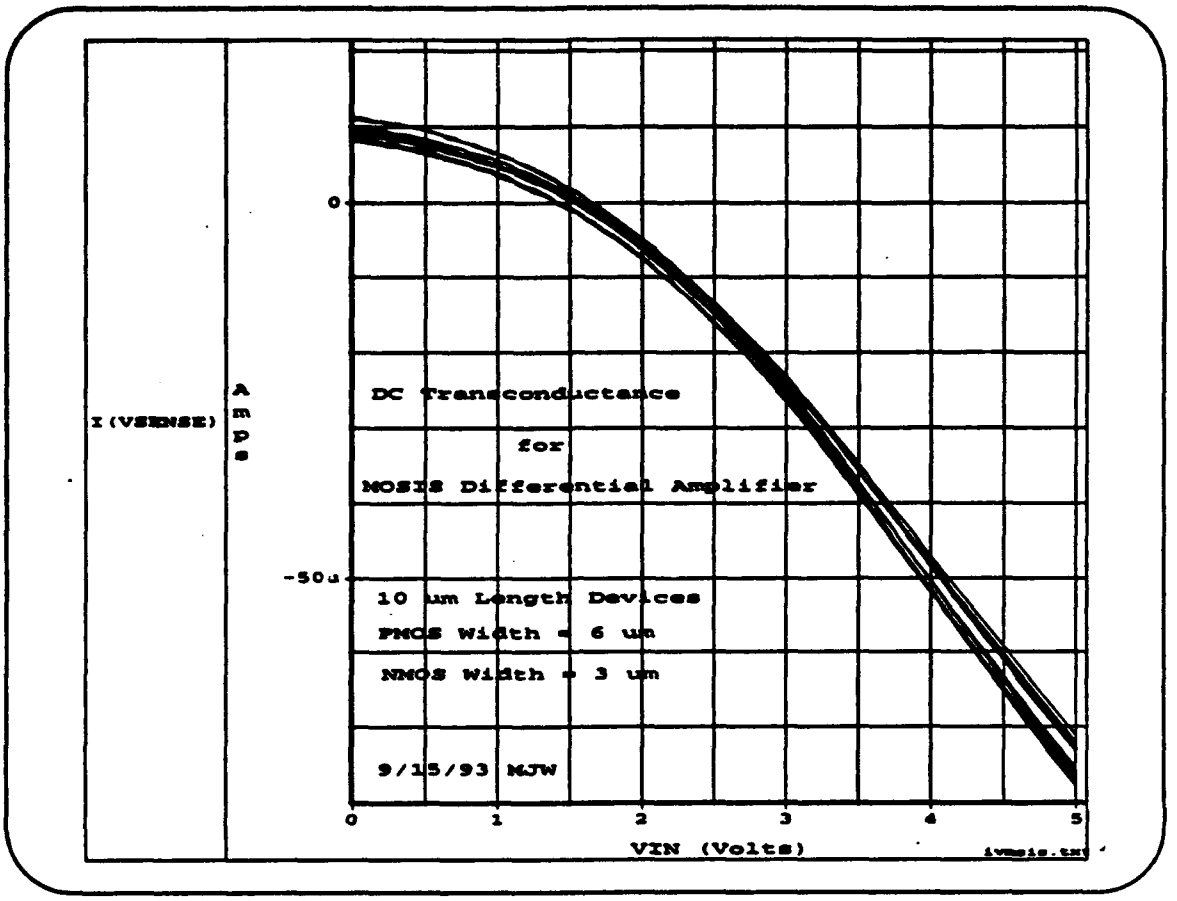

Figure 8. DC Transconductance For MOSIS Differential Amplifier L = 10 μm, W(PMOS) = 6 μm, W(NMOS) = 3 μm

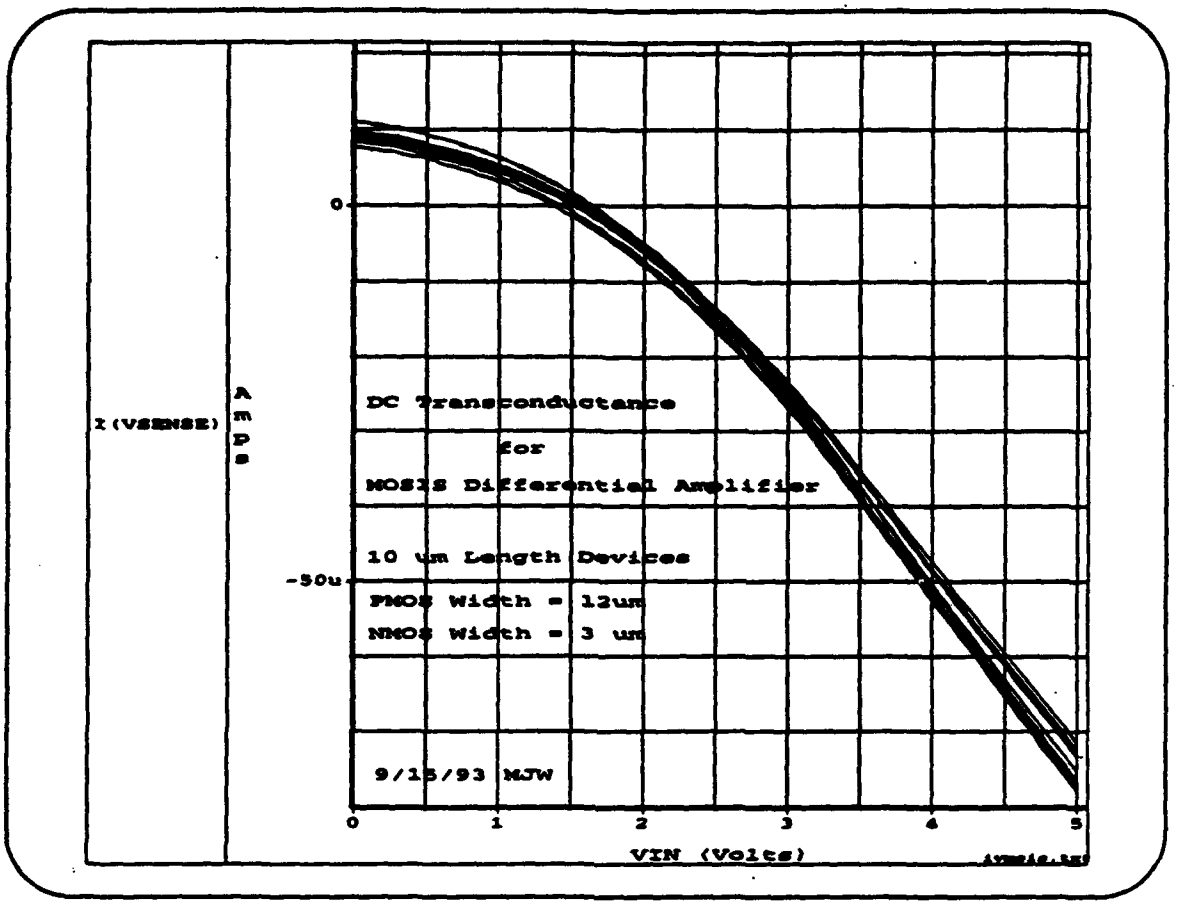

Figure 9. DC Transconductance For MOSIS Differential Amplifier L = 10 μm, W(PMOS) = 12 μm, W(NMOS) = 3 μm

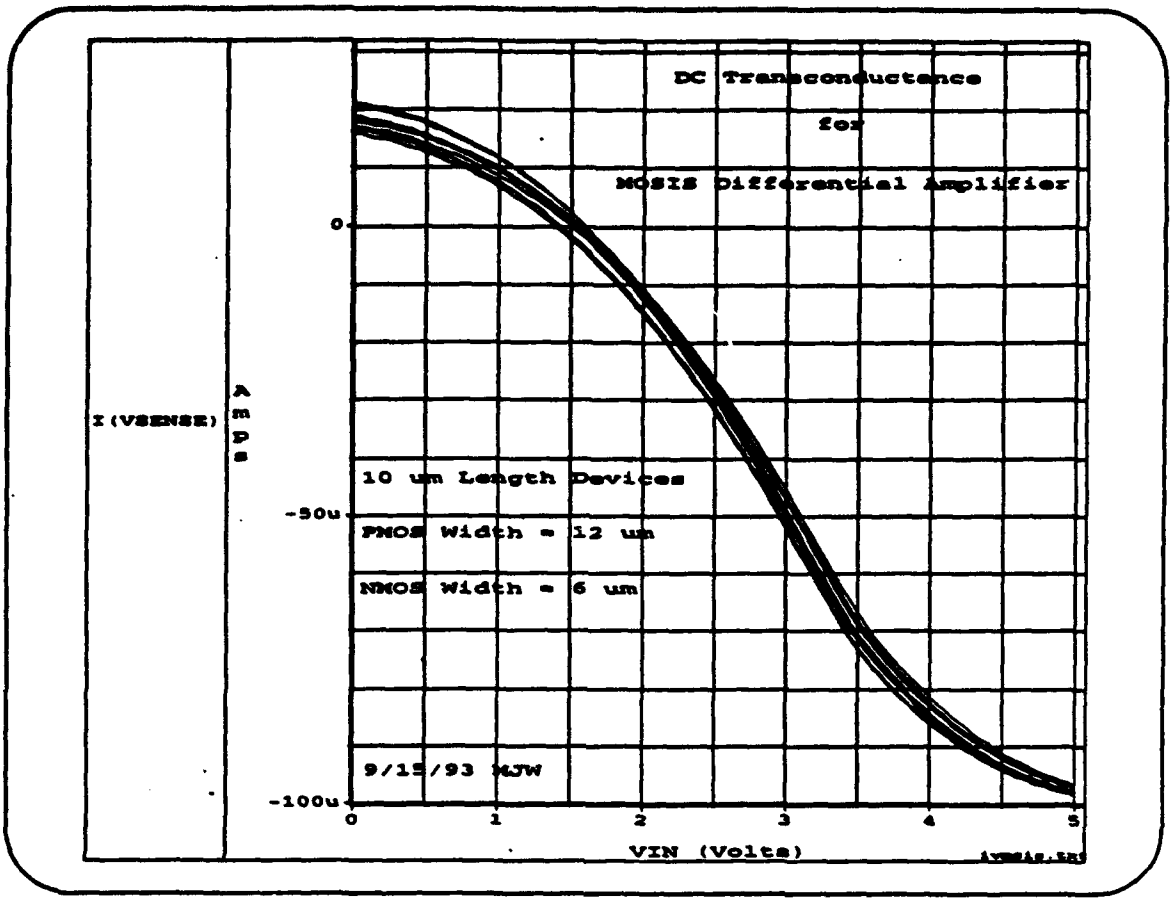

Figure 10. DC Transconductance For MOSIS Differential Amplifier L = 10 μm, W(PMOS) = 12 μm, W(NMOS) = 6 μm

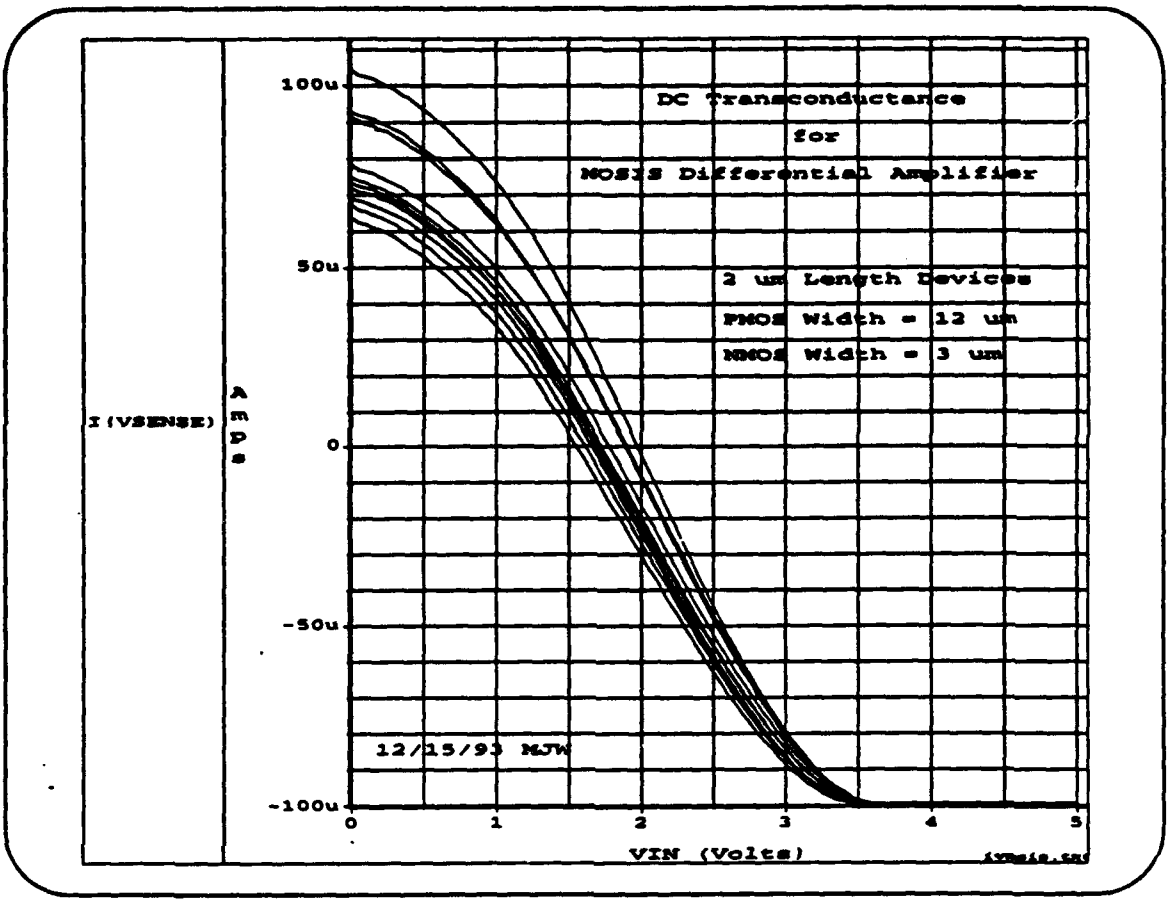

Figure 11. DC Transconductance For MOSIS Differential Amplifier L = 2 μm, W(PMOS) = 12 μm, W(NMOS) = 3 μm

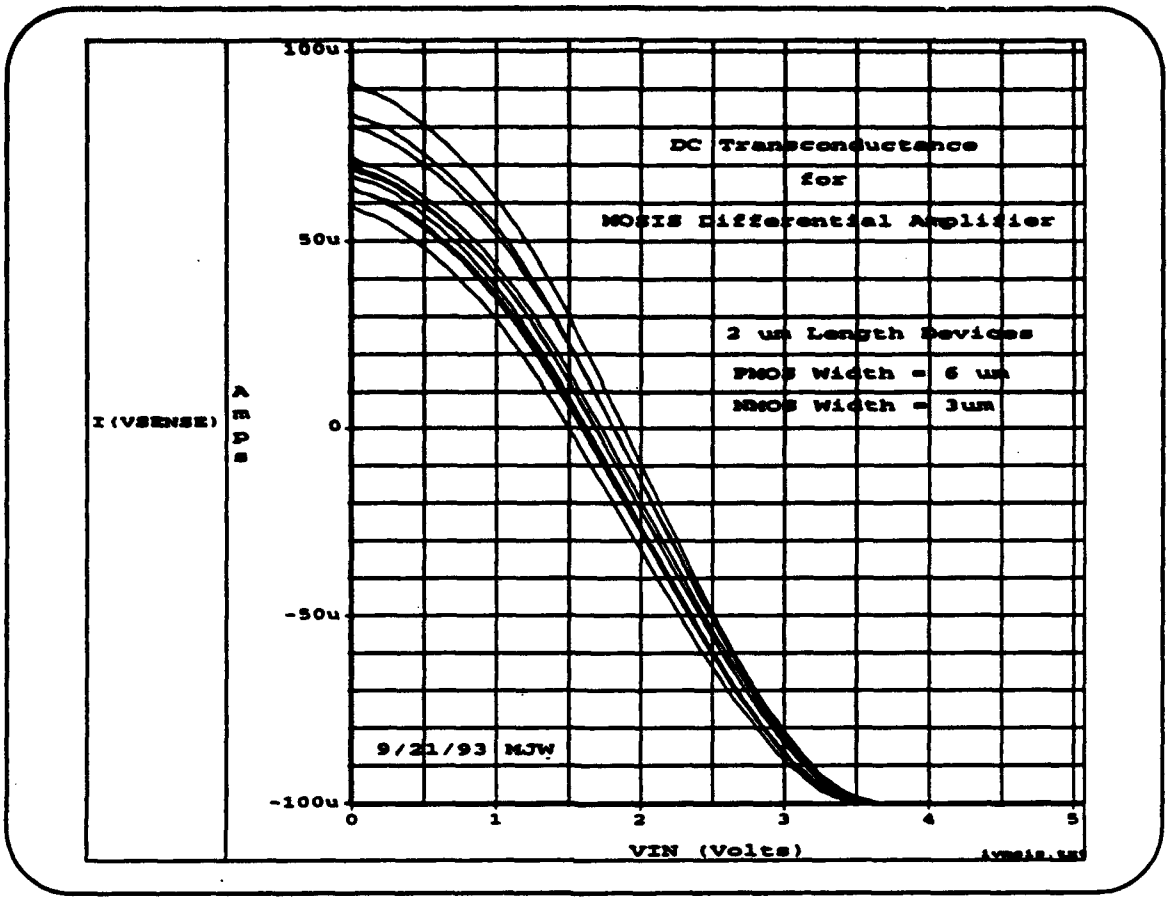

Figure 12. DC Transconductance For MOSIS Differential Amplifier L = 2 μm, W(PMOS) = 6 μm, W(NMOS) = 3 μm

The DC transconductance plots above, Figures 8 through 12, show that the process variations experienced in the MOSIS process and reflected in the device parameters do have a significant effect on DC transconductance. The fact that the plots are parallel show that small-signal transconductance is generally constant at a particular DC input voltage. Once again, the device parameter statistics that were used were gathered over time and across many wafers. Device parameter statistics might be expected to be tighter across an individual wafer.

3.7 GT PMOS Path

A differential amplifier circuit was also used for determining the circuit performance of GT PMOS devices. A schematic of this circuit is included in the results of demonstrating the methodology for GT PMOS devices. The circuit performance parameters that were chosen were large signal voltage gain, large signal transconductance, and DC supply current.

3.8 Methodology for Generating a Probability Ranked Fault Set From A Process Characterization

The following methodology assumes that a specific process description that characterizes the fabrication of a device with process parameter statistics (mean and standard deviation) is available. A flow diagram of this methodology is shown in Figure 13.

(1) Define the microelectronic fabrication process in the process simulator. This involves translating a manufacturer's process description into a form that the process simulator can understand. In addition, the process characterization should be tuned to match the SPICE parameters generated by the process simulation to those measured for the device.

(2) Determine the P critical process parameters that have the greatest effect the operation of the device. This can be done by performing a sensitivity analysis to determine the sensitivity of SPICE parameters to the various process parameters. Additionally, the equations that relate process parameters to the crucial SPICE parameters can be examined. Historical data on the process may also provide useful information. A two standard deviation variation in any one of these P process parameters will be considered a failure.

(3) Perform process simulations, mapping failures to SPICE model parameters. First, a nominal simulation should be performed as a reference in which no failures are included. Next, separate simulations for each of the P failures should be performed in which only the single failure in question is inserted. As is implicit in the previous definition of a failure, incrementing the process parameter by two standard deviations over its nominal value will constitute inserting the failure. This step is consistent with the contract requirement to consider only "singly inserted failures."

(4) Transfer the SPICE model files generated by the process simulator to the SPICE simulator. Depending on the format of the process simulator's SPICE output and the SPICE simulator's input, some translation may be necessary to convert the output into a format that the SPICE simulator can access.

(5) Perform SPICE simulations mapping SPICE models generated by the failures to circuit performance parameters. First, determine the C circuit characteristics that will be used to evaluate the microcircuit's performance. Next, nominal simulations of the microcircuit should be performed as references in which the fault-free SPICE device model is used to simulate the C circuit performance characteristics. Additionally, separate simulations using each of the P SPICE device models should be performed. For each of the P models, C SPICE simulations are performed, one for each performance characteristic. This results in a total of P times C data files that illustrate the C circuit performance characteristics for each of the P process failures. In addition, C reference data files are created that illustrate nominal circuit performance.

(6) Correlate the process failure to performance variations in the microcircuit. For each of the P process failures, the percent deviation of the C performance characteristics from the nominal can be calculated. For this calculation, the data files produced by the SPICE simulations can be examined to determine the maximum variation in circuit performance.

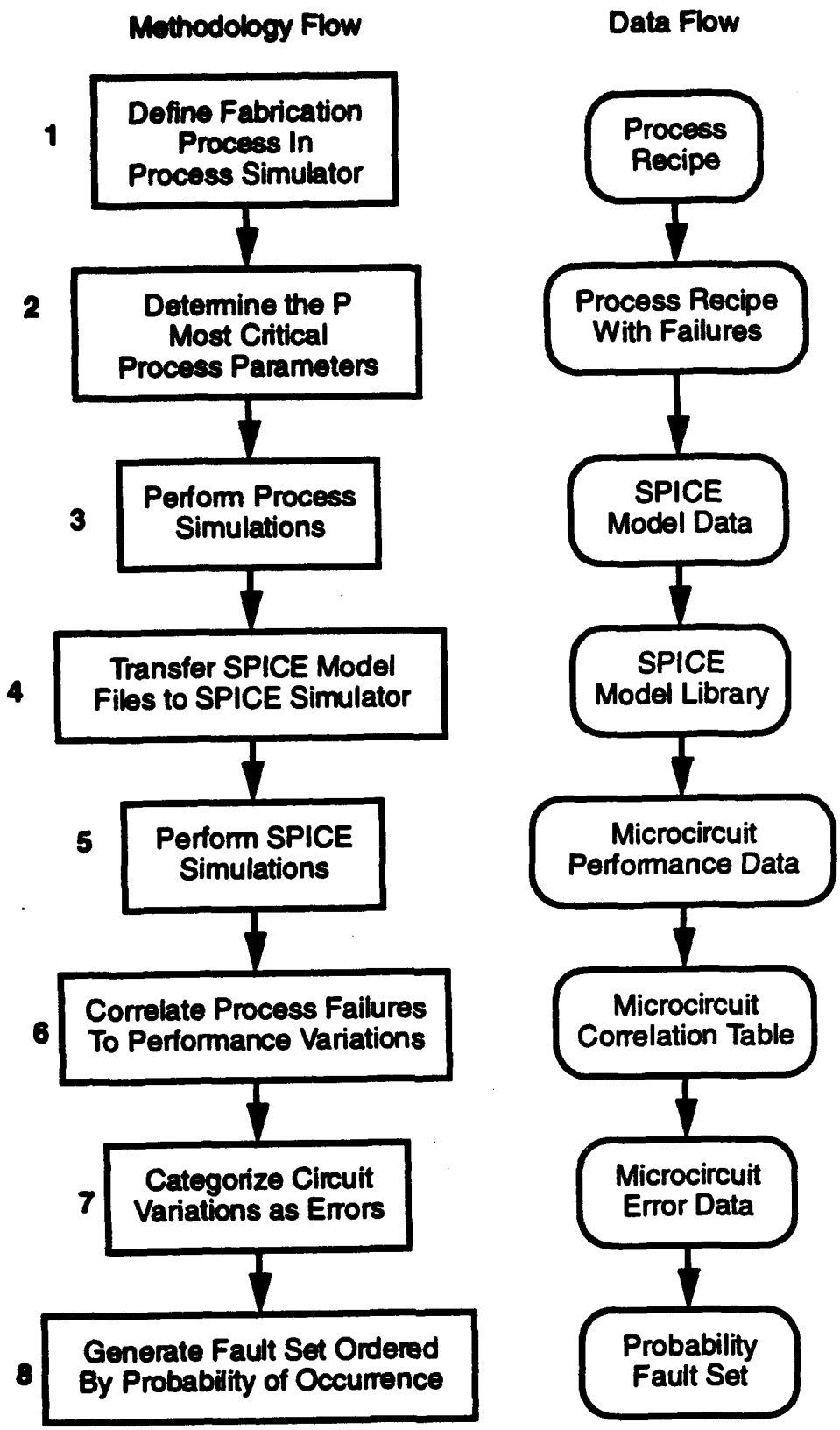

Figure 13. Methodology Flow Chart

(7) Determine which circuit variations constitute errors in the microcircuit's performance. First, define a minimum percent deviation from the norm that constitutes an error for each of C circuit performance characteristics. Next, determine by comparison to this standard which of the P process failures cause errors in the C circuit performance characteristics.

(8) Generate a fault set ordered by probability of occurrence. Given the previous definition of a failure as being a two standard deviation variation in a process parameter and assuming a normal Gaussian distribution of failures, each failure will have an equal probability of occurrence of **4.56%**. The following equations summarize the calculations necessary to determine the probability of occurrence for each of the C errors in circuit performance.

P = number of process variables that are potential failures
C = number of circuit performance characteristics

Failures:

X_1 = process variable 1
X_2 = process variable 2
•
•
•
X_P = process variable P
N = no failures
V = any failure

Probability of 2 standard deviation variation occurring:

$$P\{X_1\} = P\{X_2\} = \bullet\bullet\bullet = P\{X_P\} = \mathbf{0.0456}$$

$$P\{\overline{X}_1\} = 1 - 0.0456 = 0.9544$$

$$P\{N\} = P\{\overline{X}_1 \& \overline{X}_2 \& \bullet\bullet\bullet \& \overline{X}_P\} = P\{\overline{X}_1\} x P\{\overline{X}_2\} x \bullet\bullet\bullet x P\{\overline{X}_P\} = (0.9544)^P$$

Probability of at least one failure occurring:

$$P\{V\} = 1 - P\{N\} = 1 - (0.9544)^P$$

C possible errors assumed:

$$E_1, E_2, \bullet\bullet\bullet, E_C$$

The probability of an error given a specific failure occurs (from simulated data):

E_1:

$$P\{E_1|X_1\} = ?\ (0 \text{ or } 1)$$
$$P\{E_1|X_2\} = ?\ (0 \text{ or } 1)$$
$$\vdots$$
$$P\{E_1|X_P\} = ?\ (0 \text{ or } 1)$$

E_C:

$$P\{E_C|X_1\} = ?\ (0 \text{ or } 1)$$
$$P\{E_C|X_2\} = ?\ (0 \text{ or } 1)$$
$$\vdots$$
$$P\{E_C|X_P\} = ?\ (0 \text{ or } 1)$$

The probability of an error given at least one failure occurs:

$$P\{E_1|V\} = (\text{number of faults that cause } E_1)/P$$
$$\vdots$$
$$P\{E_C|V\} = (\text{number of faults that cause } E_C)/P$$

The probability of each error (the probability ranked fault set):

$$P\{E_1\} = P\{E_1|V\} \times P\{V\}$$
$$\vdots$$
$$P\{E_C\} = P\{E_C|V\} \times P\{V\}$$

3.9 Results of Demonstrating Methodology With GT PMOS Process

Because there was no statistical data for the Georgia Tech PMOS process, the available nominal data was used with an assumed 5 % standard deviation. A specific process description was also available. In this case the process simulator was PREDITOR and the SPICE simulator was PSPICE.

(1) The process description was entered into PREDITOR using the built in process editing capability. Extensive tuning of the process characterization was necessary to more closely match the SPICE parameters generated by the process simulation to the measured parameters summarized in Table 1. The resulting process flow is described in Appendix B.

(2) From a sensitivity analysis performed in PREDITOR, six critical process parameters (P = 6) were determined. The equations that relate process parameters to the critical SPICE parameters verified the selection of these parameters. These parameters included: the temperature during the gate oxide growth, the temperature during the boron predeposition, the source concentration used during the boron predeposition, the metal thickness deposition rate, the temperature during the metal deposition, and the gate oxide charge density (Qss).

(3) A nominal simulation for reference and six additional simulations for each of the P = 6 failures were performed in PREDITOR. A two standard deviation variation, corresponding to a 10% increase from the nominal value, was used to model failures in each of the six critical process parameters. This resulted in a total of seven text files containing SPICE model data. Transfer curves and a source/drain doping profile from the nominal PREDITOR simulation are found in Figures 14 and 15.

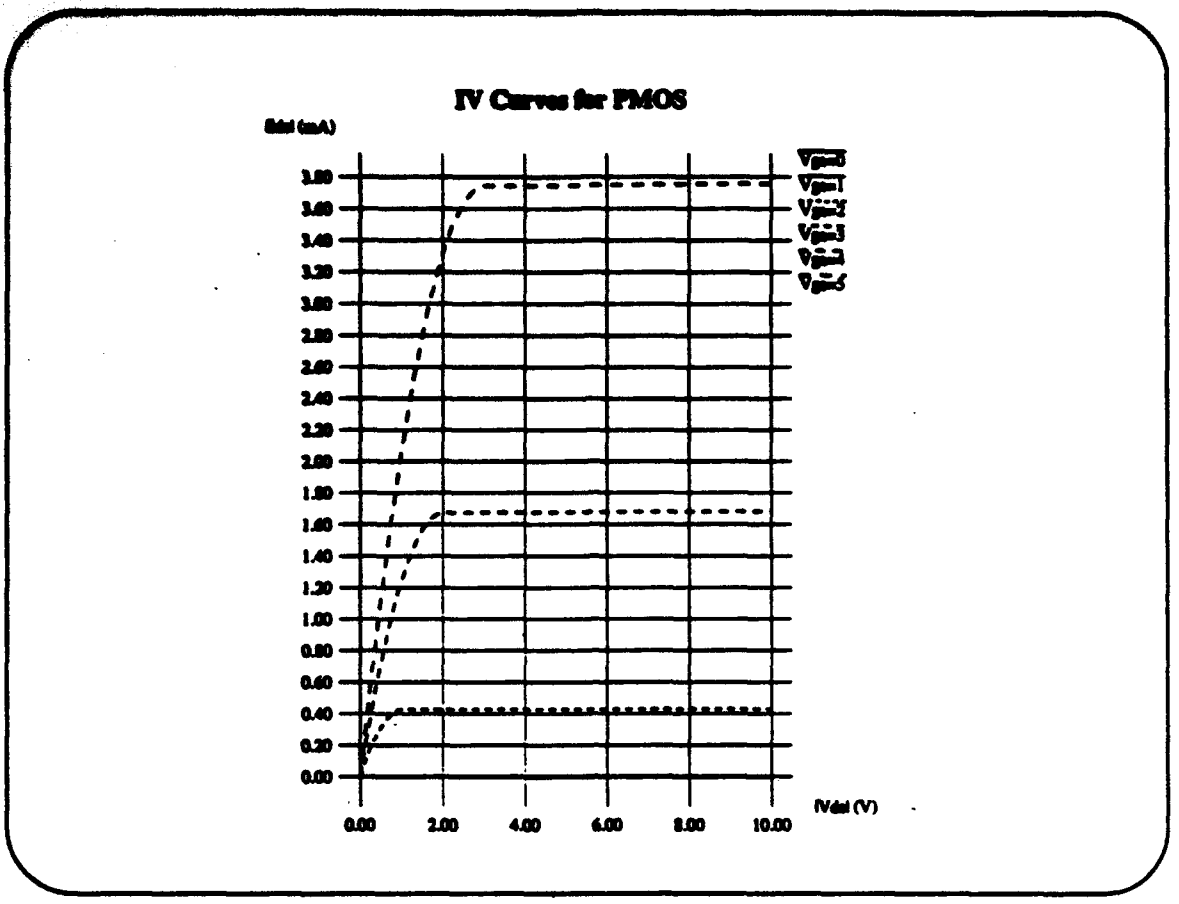

Figure 14. Plot of PMOS Transfer Characterization From PREDITOR

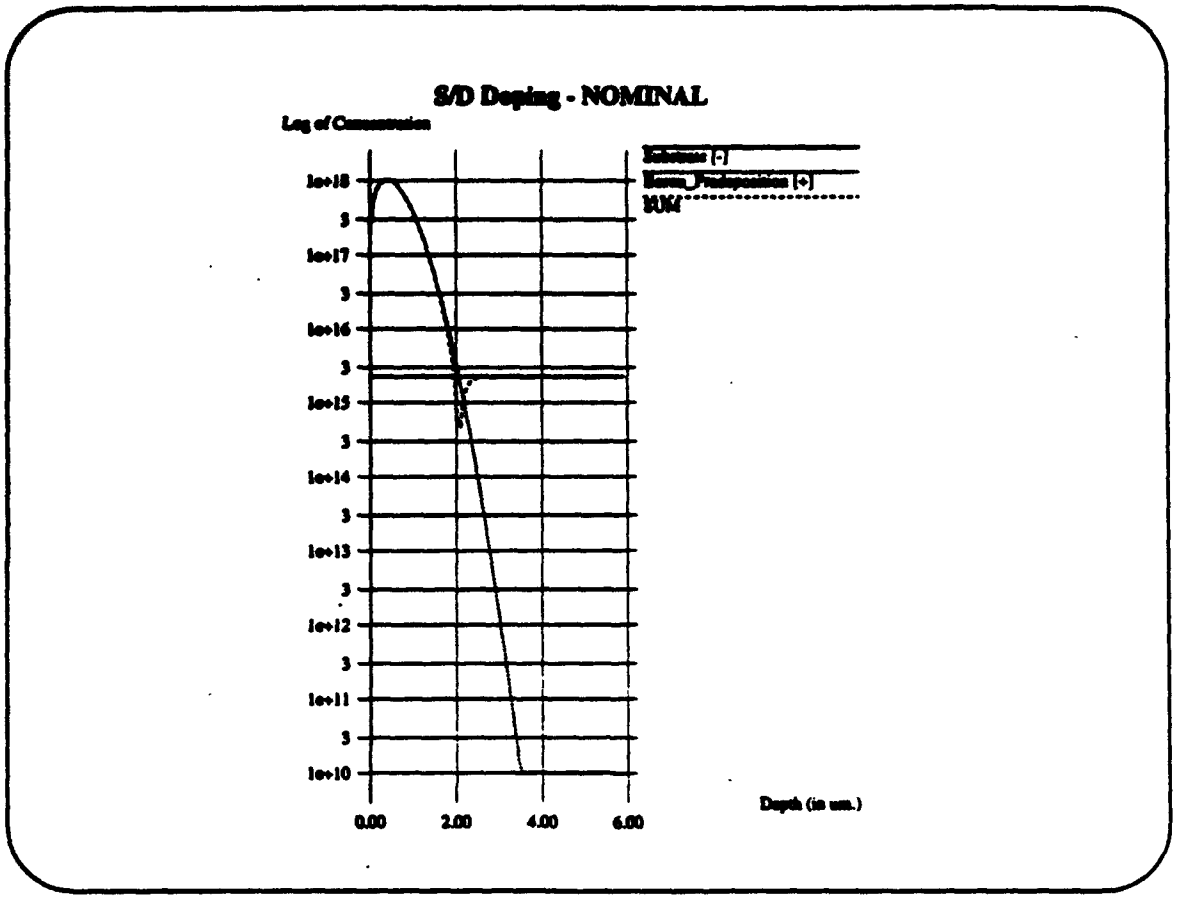

Figure 15. Plot of Source/Drain Doping Profile From PREDITOR

(4) Because the SPICE2 output from PREDITOR was not exactly standard SPICE, some changes were made to create the PMOS and NMOS model files to be used by PSPICE. In particular, the PMOS model data generated by the process simulation was duplicated as an accompanying NMOS transistor model with VT0 as a positive value for the NMOS parameter and with VT0 as a negative value for the PMOS parameter. A library file containing all seven NMOS and PMOS models was created for use by PSPICE.

(5) For the microcircuit found in Figures 16 and 17, two characteristics (C = 2), large signal transconductance and large signal voltage gain, were used to evaluate the microcircuits's performance. In order to graphically compare the performance of the microcircuit containing process failure devices to the nominal microcircuit, two circuits were simultaneously simulated as shown in Figures 16 and 17.

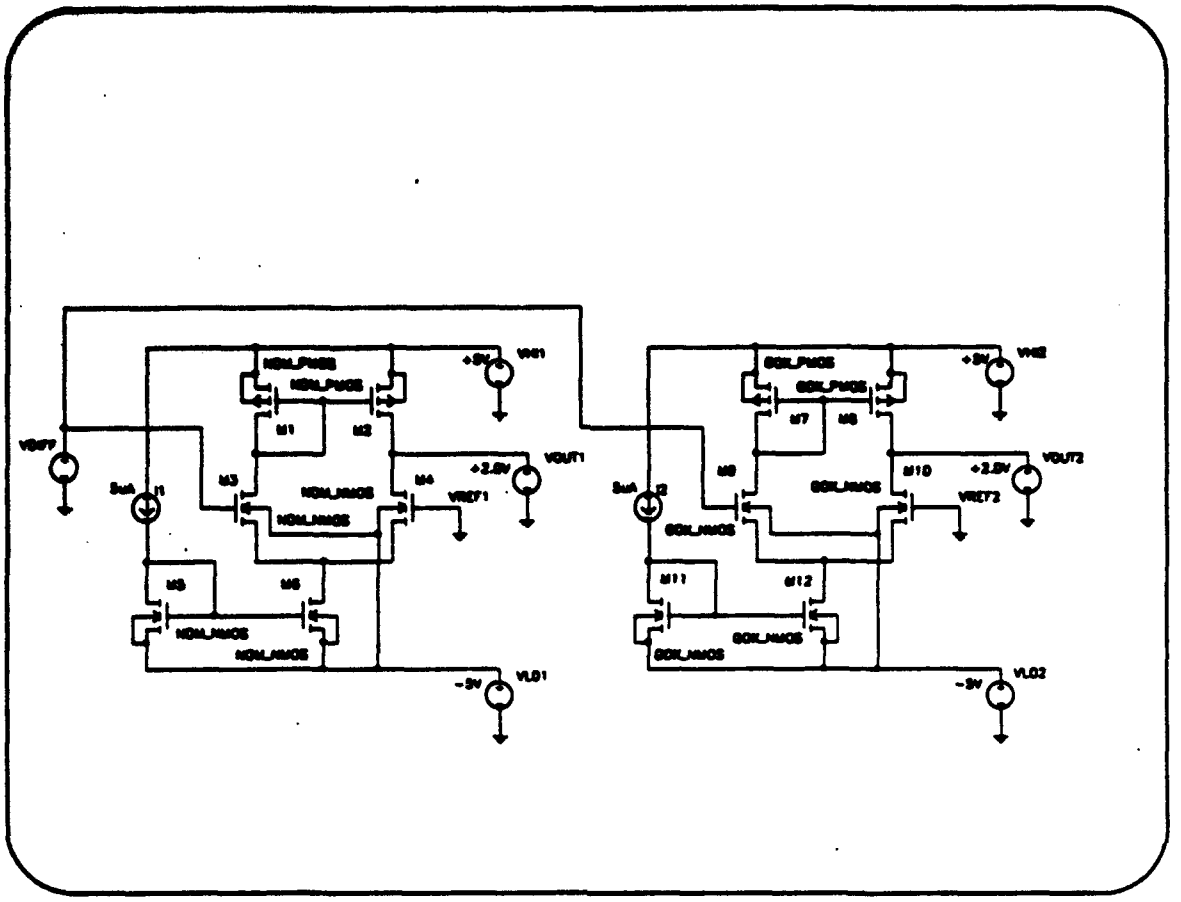

Figure 16. Schematic for Large Signal Transconductance Simulation

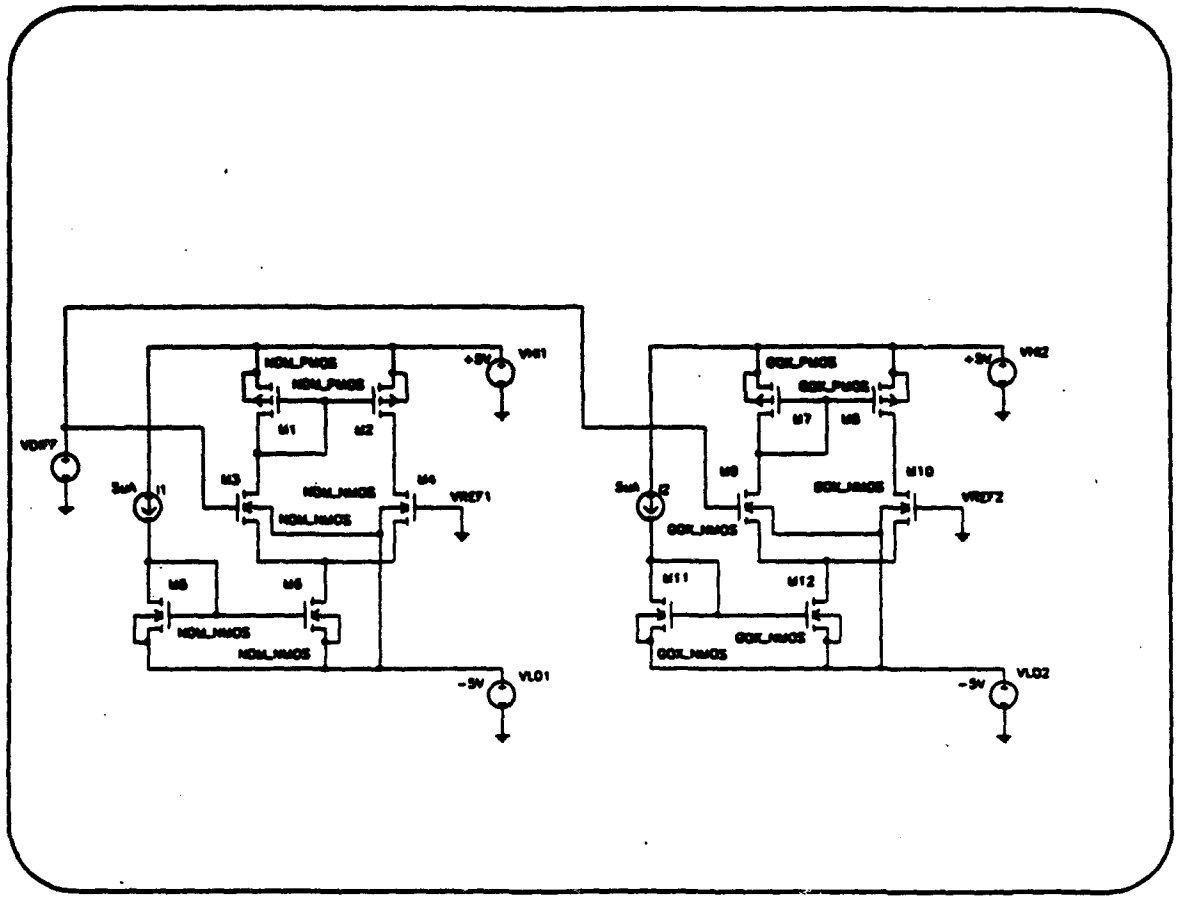

Figure 17. Schematic for Large Signal Voltage Gain Simulation

For each of the P = 6 models, both SPICE simulations were performed , one for each performance characteristic. This resulted in a total of P = 6 times C = 2 data files (total = 12) that illustrate the two circuit performance characteristics for each of the six process failures in relation to the nominal performance. Normal I-V and V-V plots were created along with the derivative of the current and voltage out with respect to the input voltage. Plots of power supply current drain were also generated to examine another possible error. The following graphs summarize the PSPICE simulation results.

The first process variation involved a ten percent change in the temperature during the gate oxide growth from 1100 degrees C to 1210 degrees C. This leads to an increase in the gate oxide thickness from 0.10 microns to 0.16 microns. The resulting transconductance characterization is found in Figures 18 and 19.

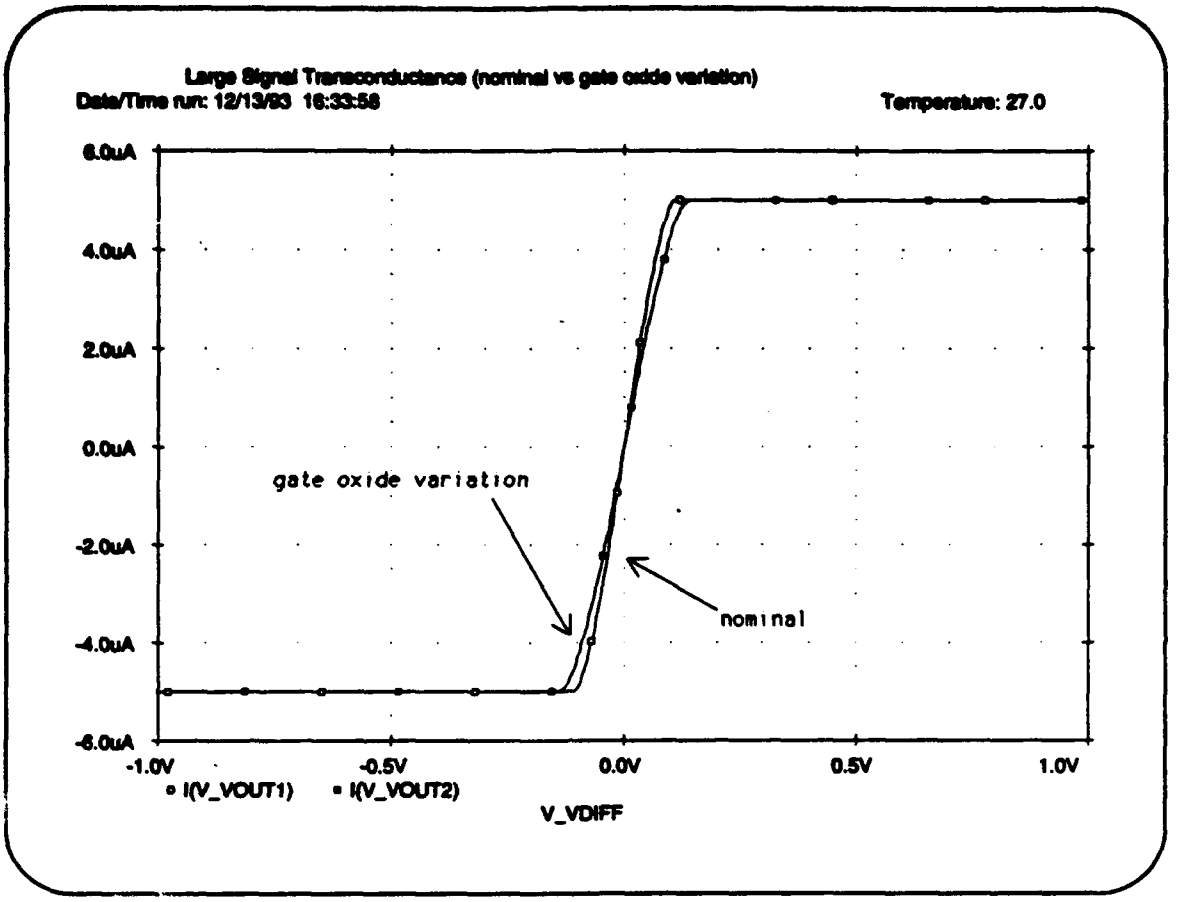

Figure 18. Gox Process Variation Effect on Large Signal Transconductance

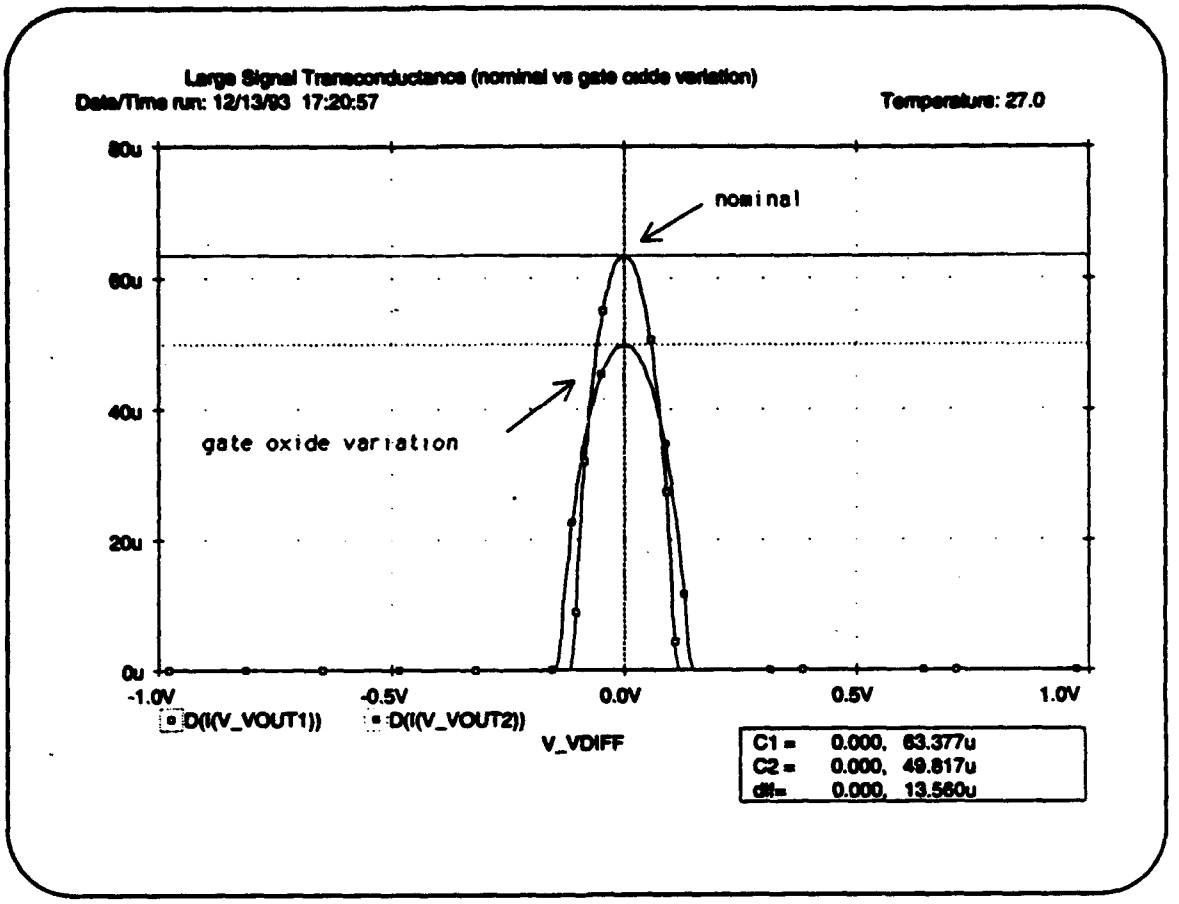

Figure 19. Gox Process Variation Effect on Large Signal Transconductance (Derivative)

From Figure 19 we note a **21.4%** drop in the maximum transconductance from the nominal value of 63.377 microSiemens to 49.817 microSiemens. The voltage gain characterization is found in Figures 20 and 21.

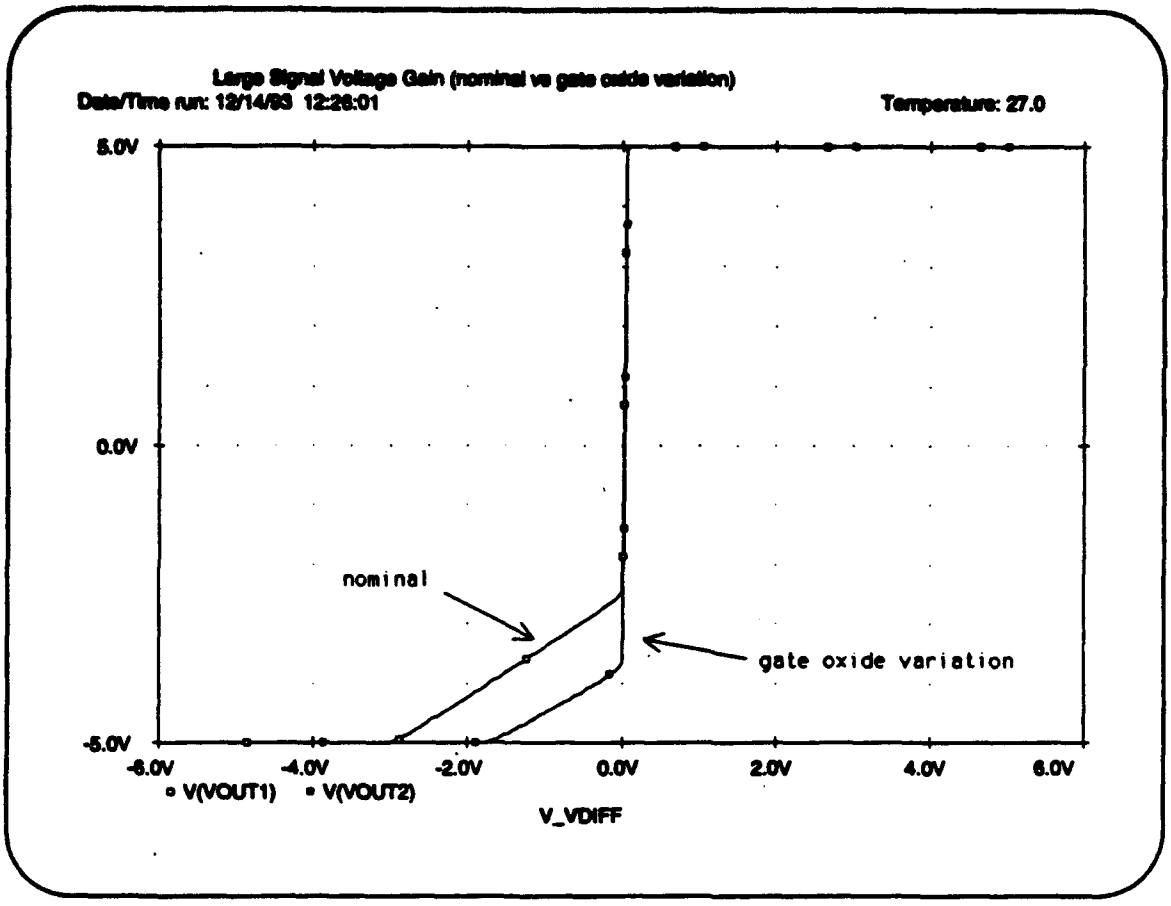

Figure 20. Gox Process Variation Effect on Large Signal Voltage Gain

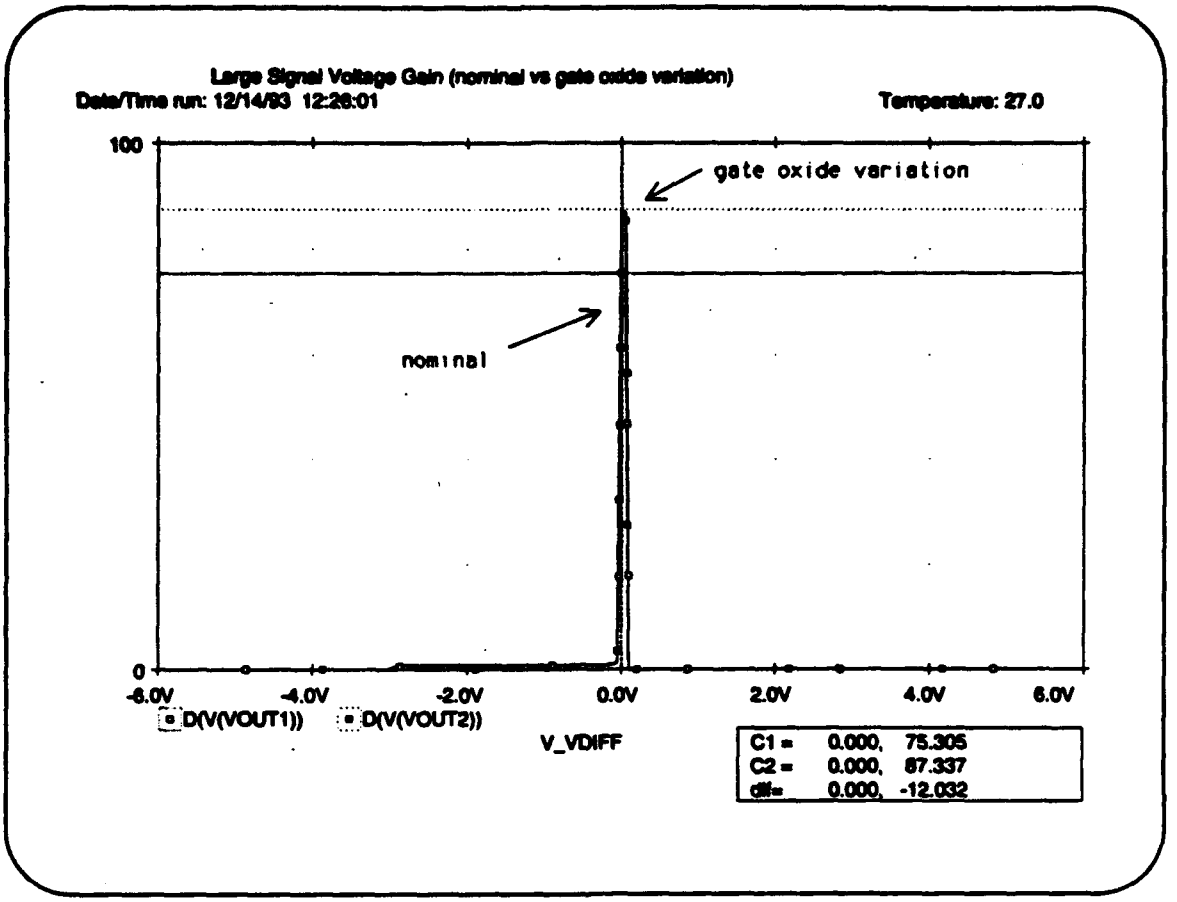

Figure 21. Gox Process Variation Effect on Large Signal Voltage Gain (Derivative)

From Figure 21 we note a **16.0%** rise in the maximum voltage gain from the nominal value of 75.305 V/V to 87.337 V/V. The power supply current drain characterization for the voltage gain simulation is found in Figure 22.

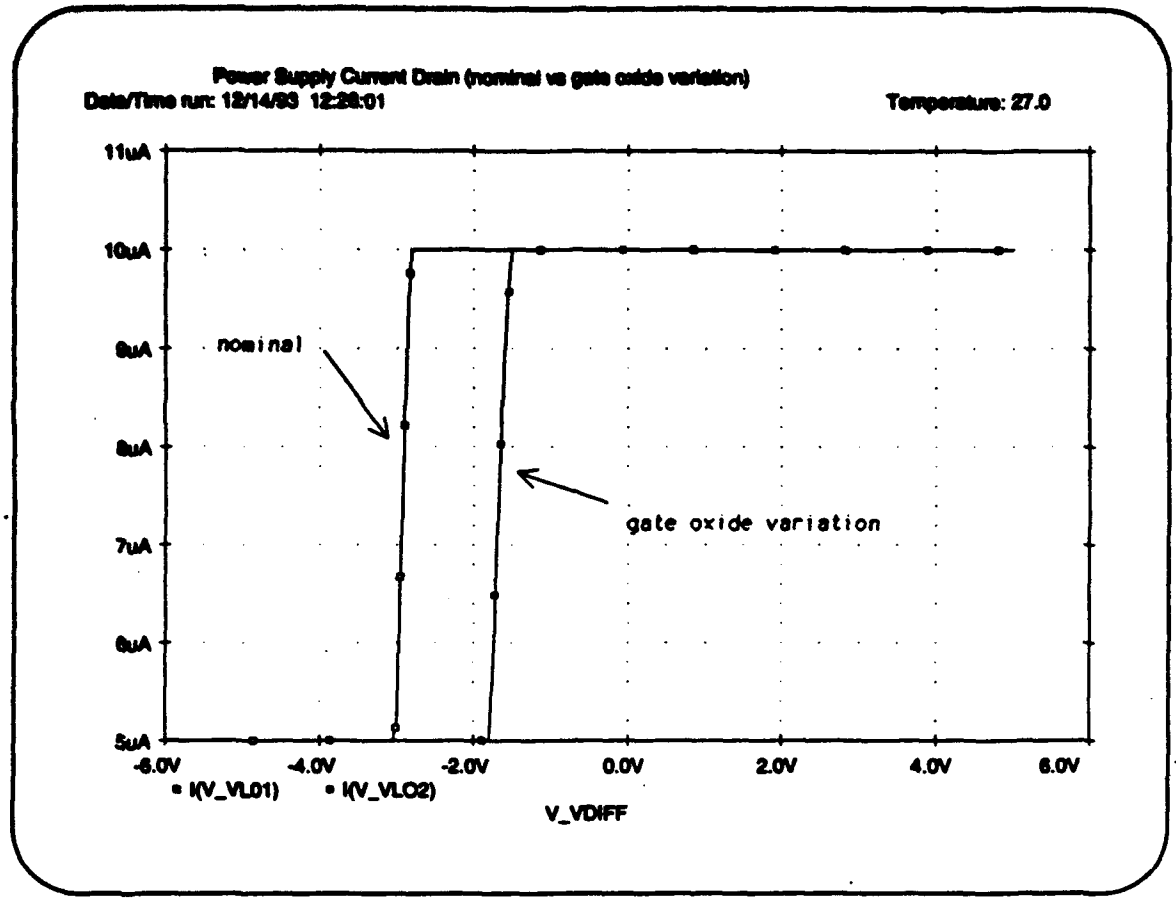

Figure 22. Gox Variation Effect on Power Supply Current Drain

From this graph we note approximately a one volt difference in the point at which the supply current rose from 5 microamps to 10 microamps.

The second process variation involved a ten percent change in the temperature during the boron predeposition from 1100 degrees C to 1210 degrees C. This led to a change in the source/drain doping profile as seen in Figure 23.

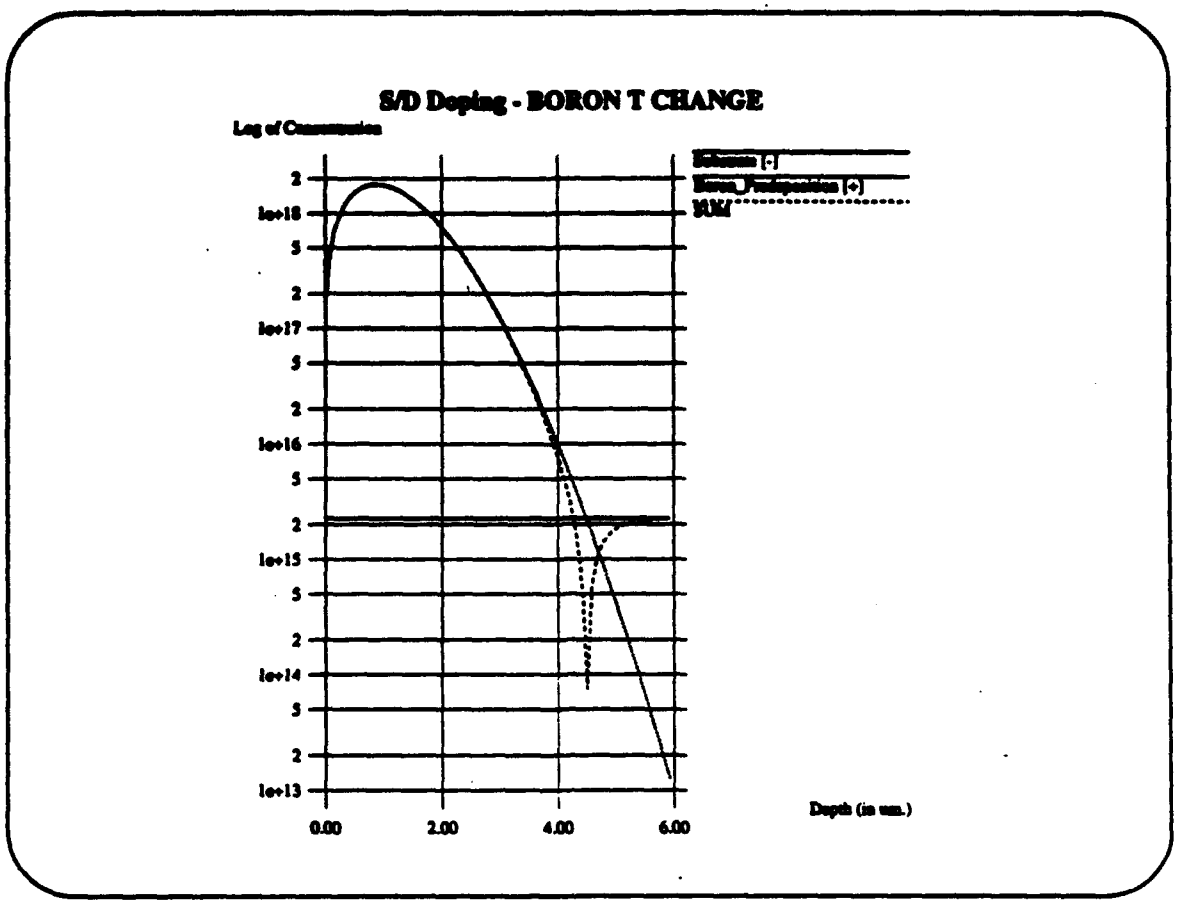

Figure 23. Plot of Source/Drain Doping Profile From PREDITOR

The resulting transconductance characterization is found in Figures 24 and 25.

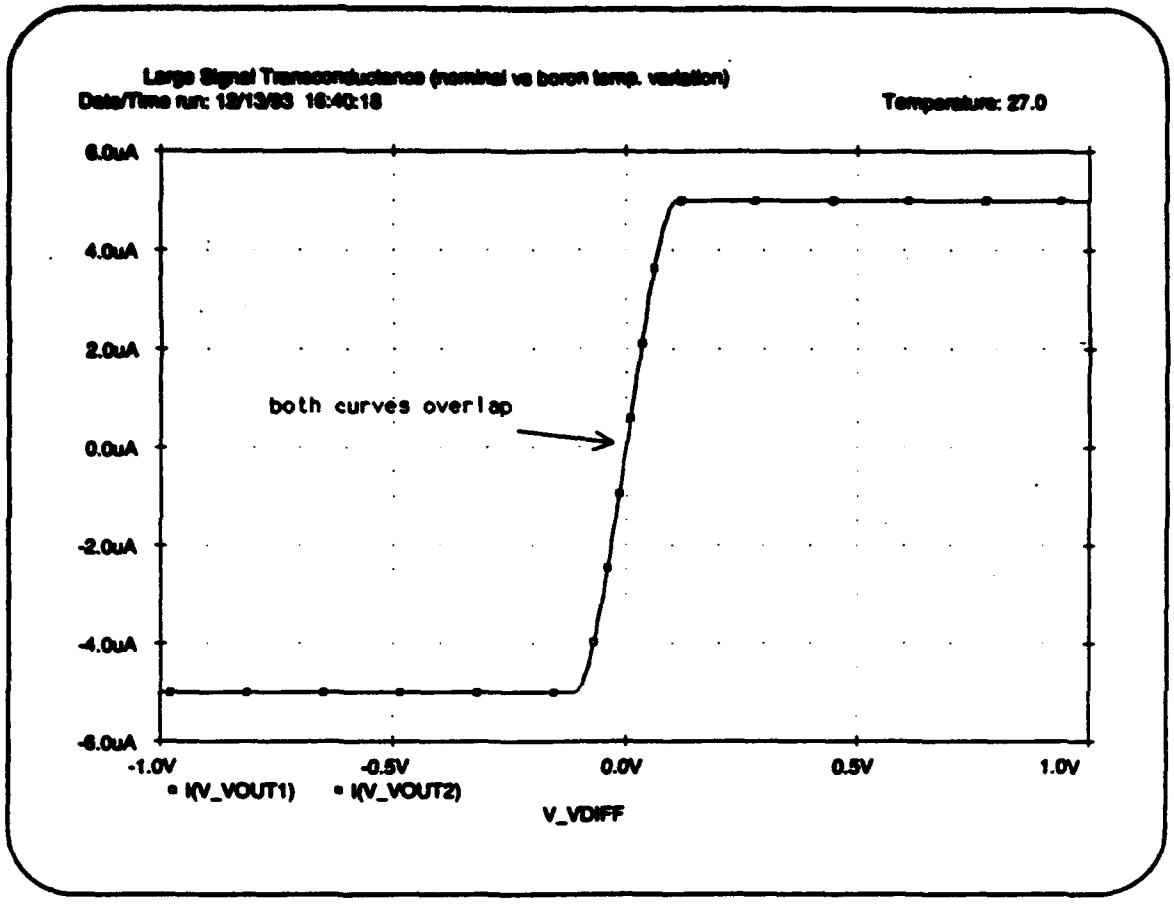

Figure 24. Boron Temperature Process Variation Effect on Large Signal Transconductance

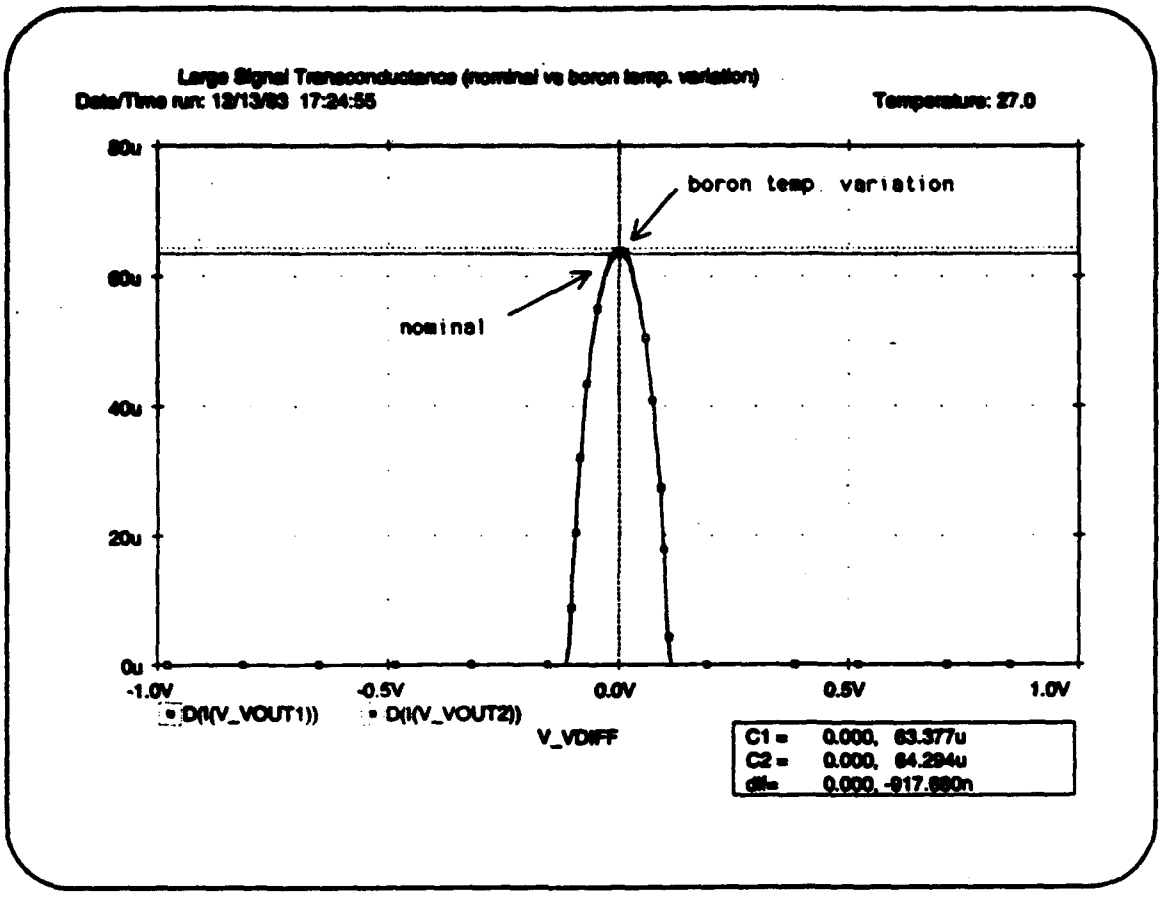

Figure 25. Boron Temperature Process Variation Effect on Large Signal Transconductance (Derivative)

From Figure 25 we note a **1.45%** rise in the maximum transconductance from the nominal value of 63.377 microSiemens to 64.294 microSiemens. The voltage gain characterization is found in Figures 26 and 27.

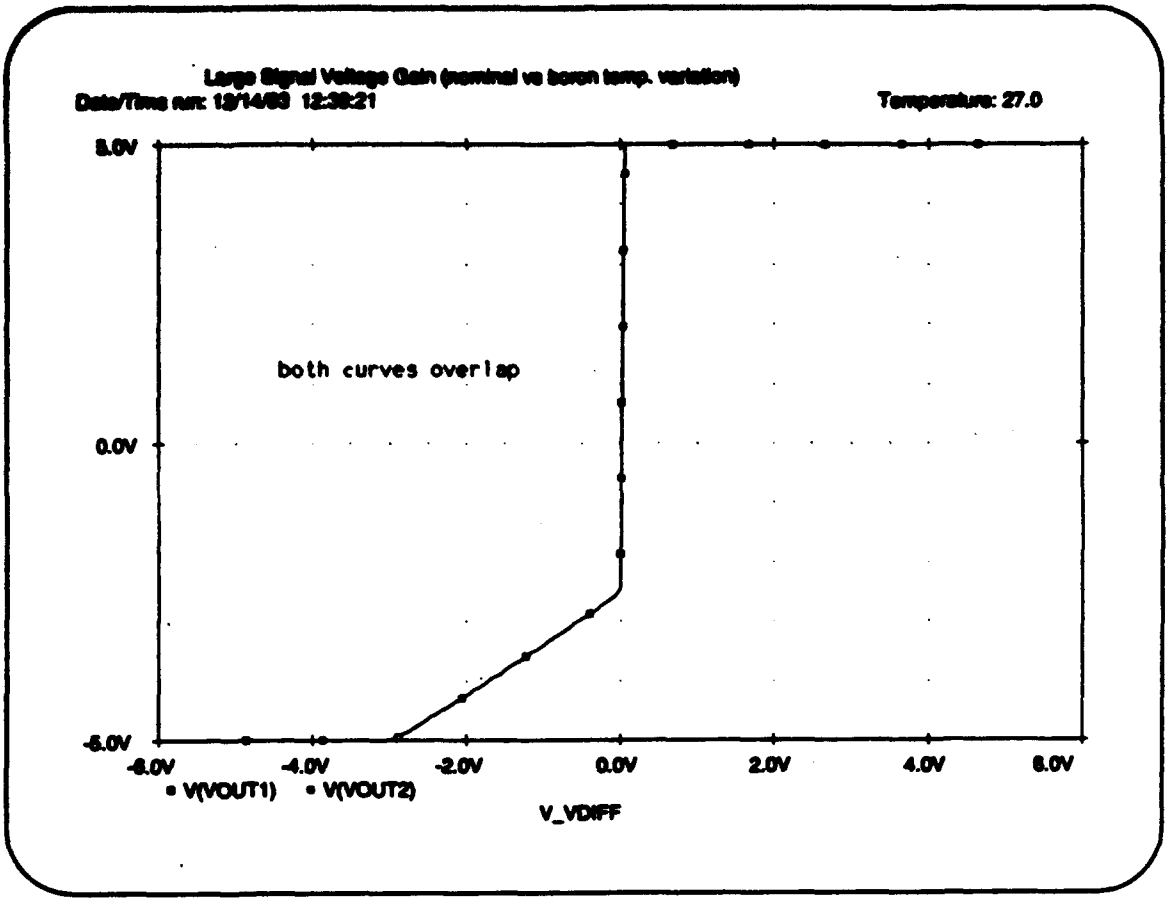

Figure 26. Boron Temperature Process Variation Effect on Large Signal Voltage Gain

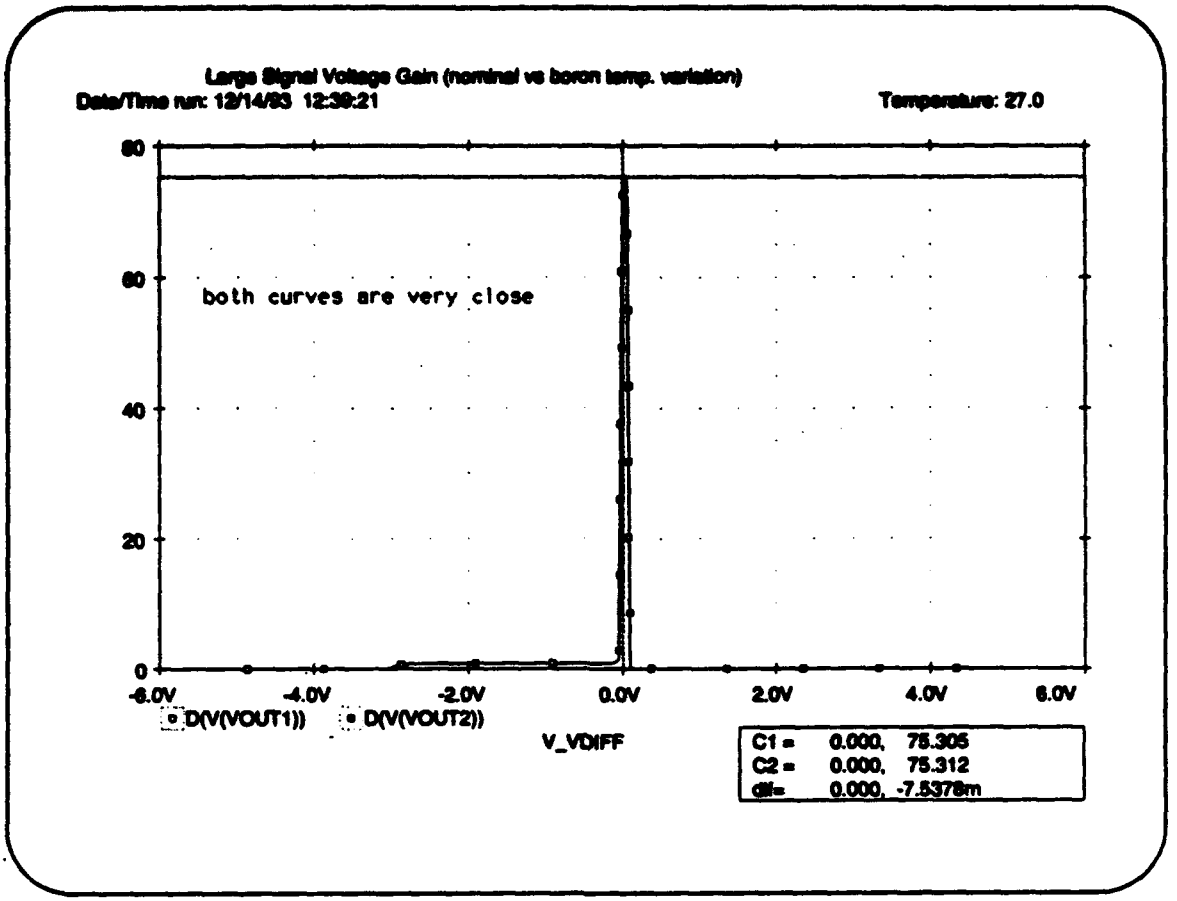

Figure 27. Boron Temperature Process Variation Effect on Large Signal Voltage Gain (Derivative)

From Figure 27 we note a **0.01%** rise in the maximum voltage gain from the nominal value of 75.305 V/V to 75.312 V/V. The power supply current drain characterization for the voltage gain simulation is found in Figure 28.

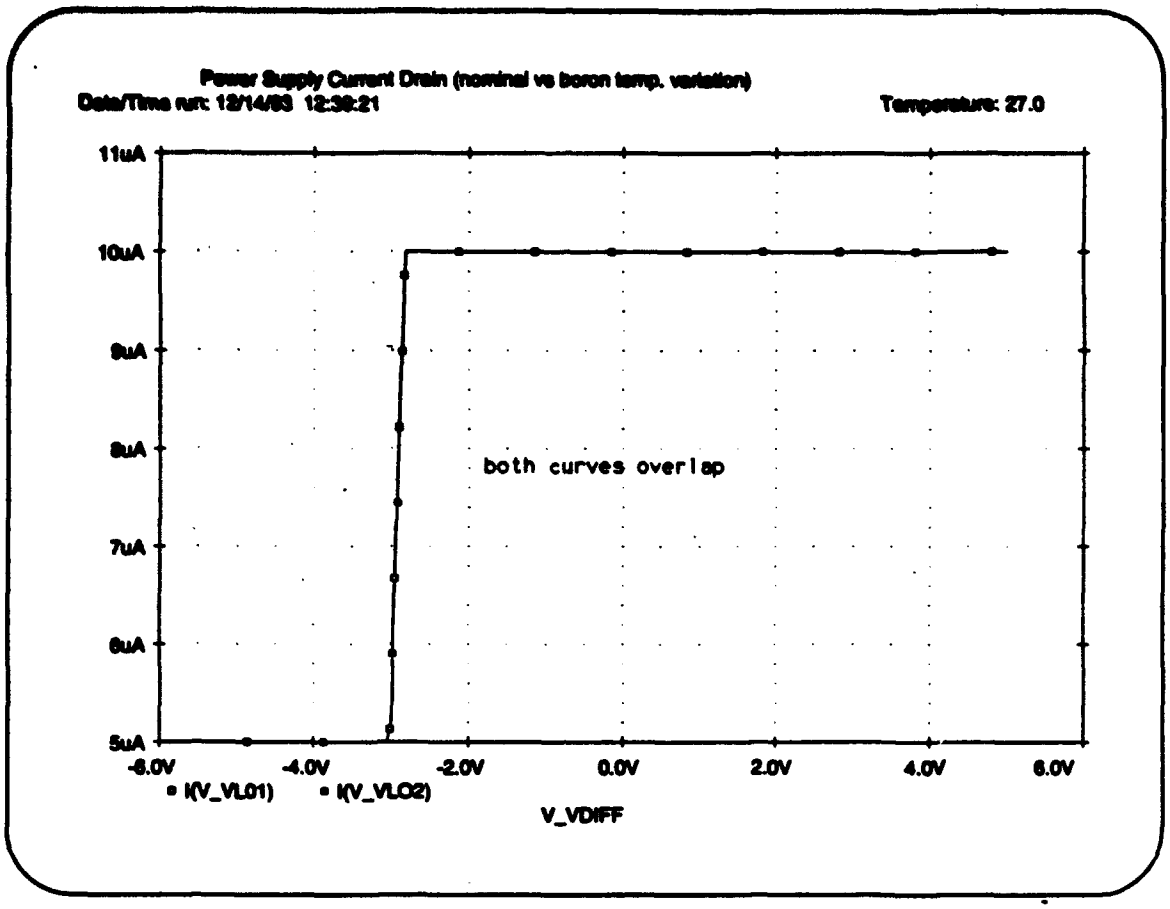

Figure 28. Boron Temperature Variation Effect on Power Supply Current Drain

From this graph we see no noticeable difference in the nominal and varied curves.

The third process variation involved a ten percent change in the boron source concentration during the boron predeposition from 1E19 cm-3 to 1.1E19 cm-3. This led to a change in the source/drain doping profile as seen in Figure 29.

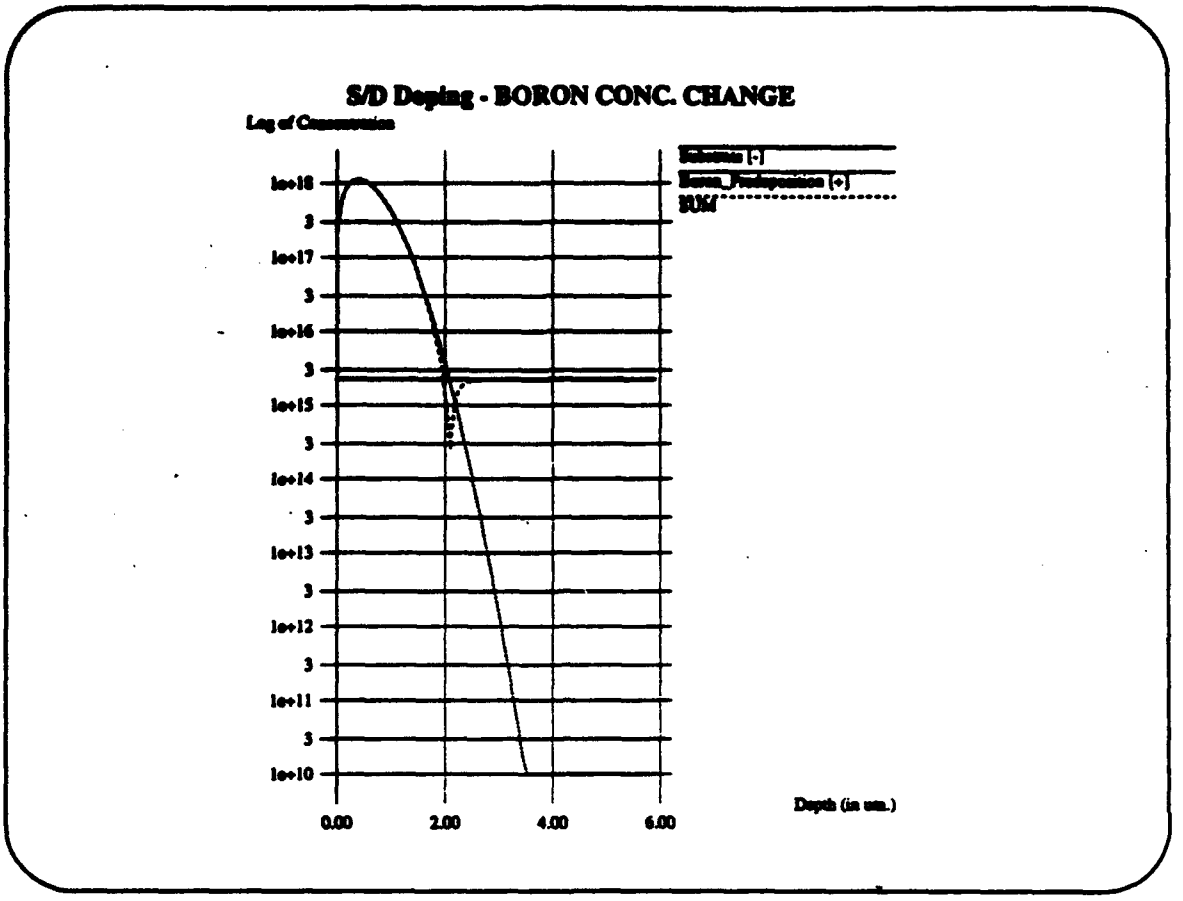

Figure 29. Plot of Source/Drain Doping Profile From PREDITOR

The resulting transconductance characterization is found in Figures 30 and 31.

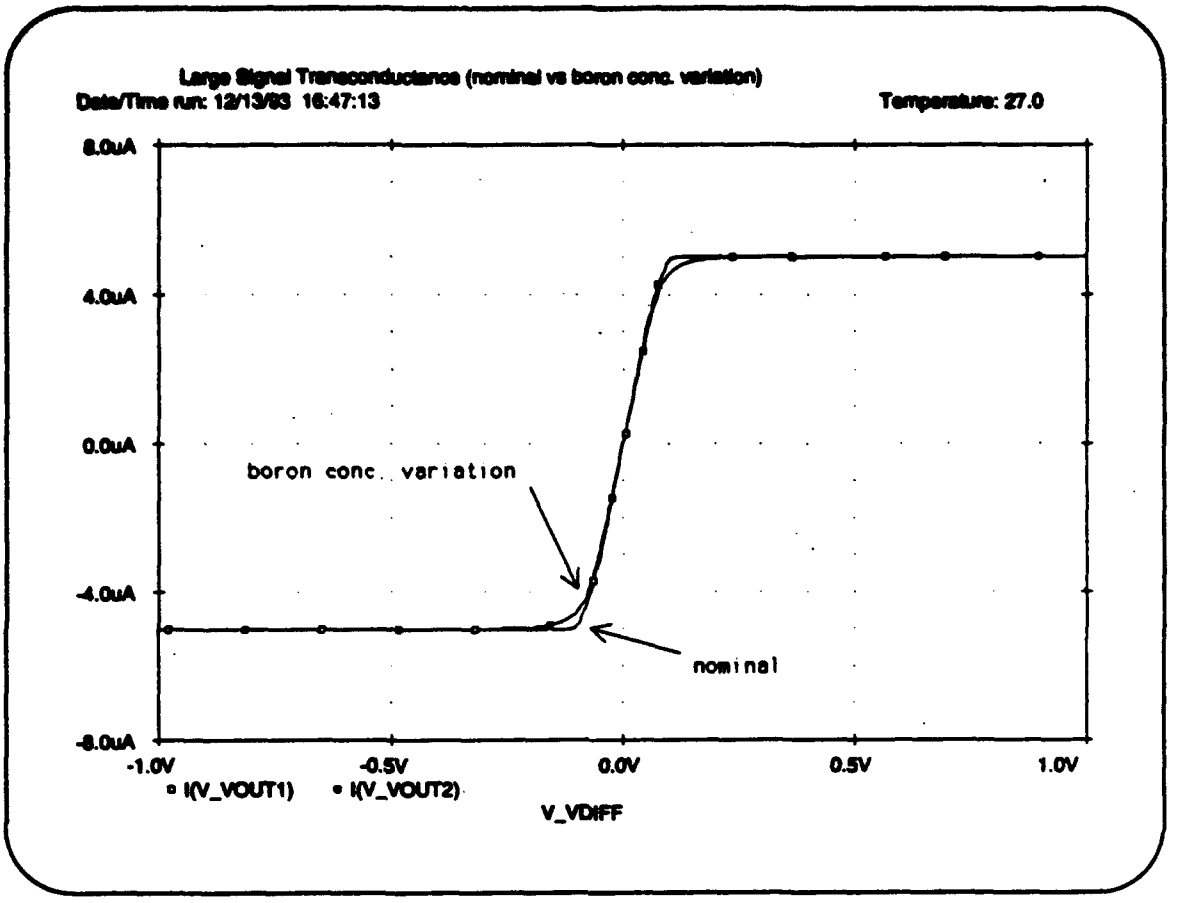

Figure 30. Boron Concentration Process Variation Effect on Large Signal Transconductance

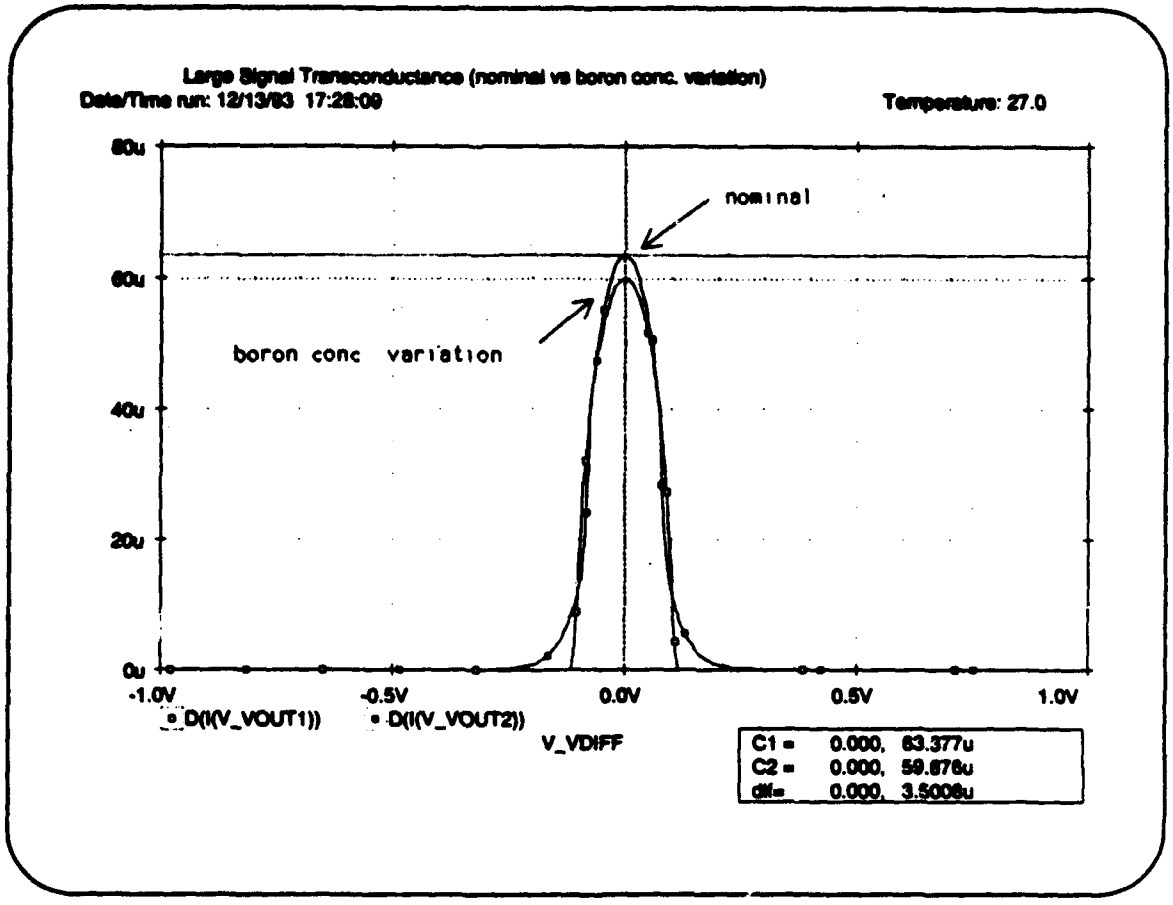

Figure 31. Boron Concentration Process Variation Effect on Large Signal Transconductance (Derivative)

From Figure 31 we note a **5.52%** drop in the maximum transconductance from the nominal value of 63.377 microSiemens to 59.876 microSiemens. The voltage gain characterization is found in Figures 32 and 33.

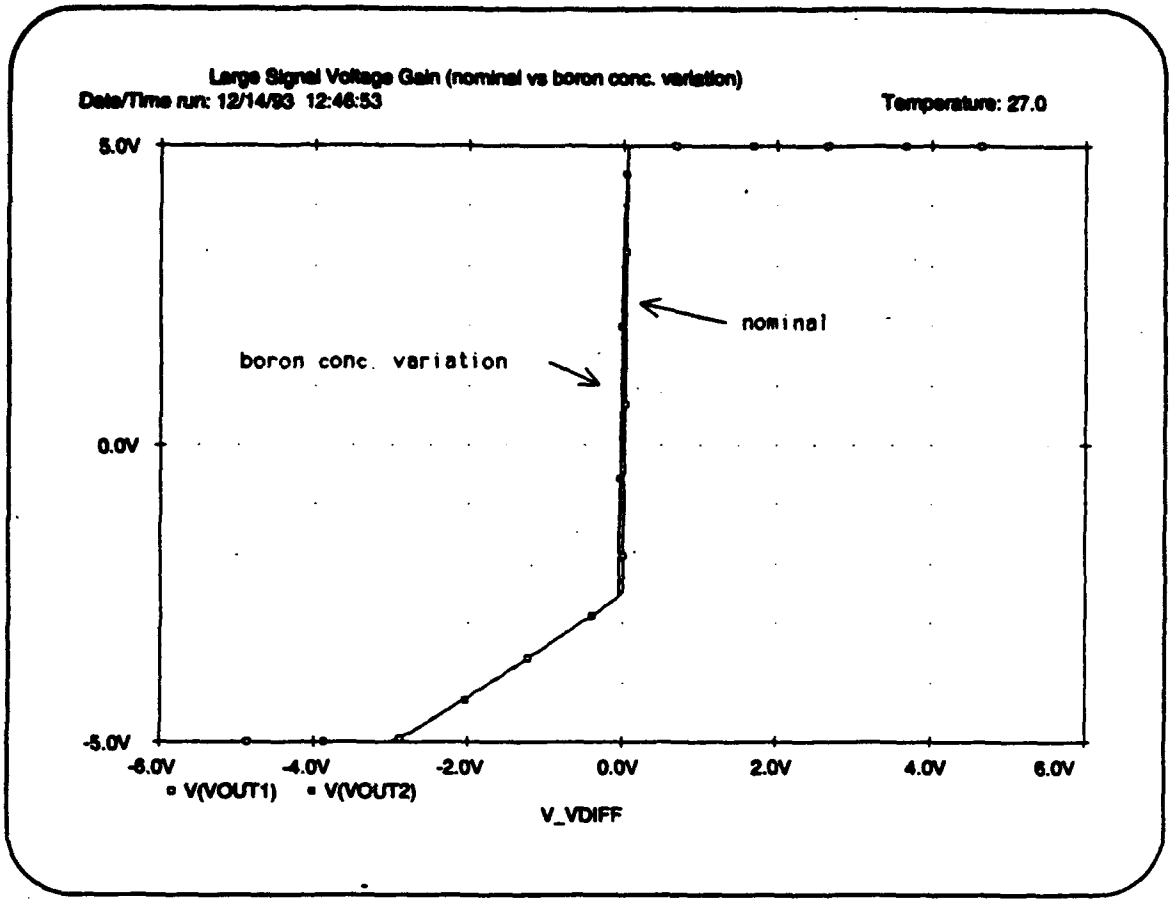

Figure 32. Boron Concentration Process Variation Effect on Large Signal Voltage Gain

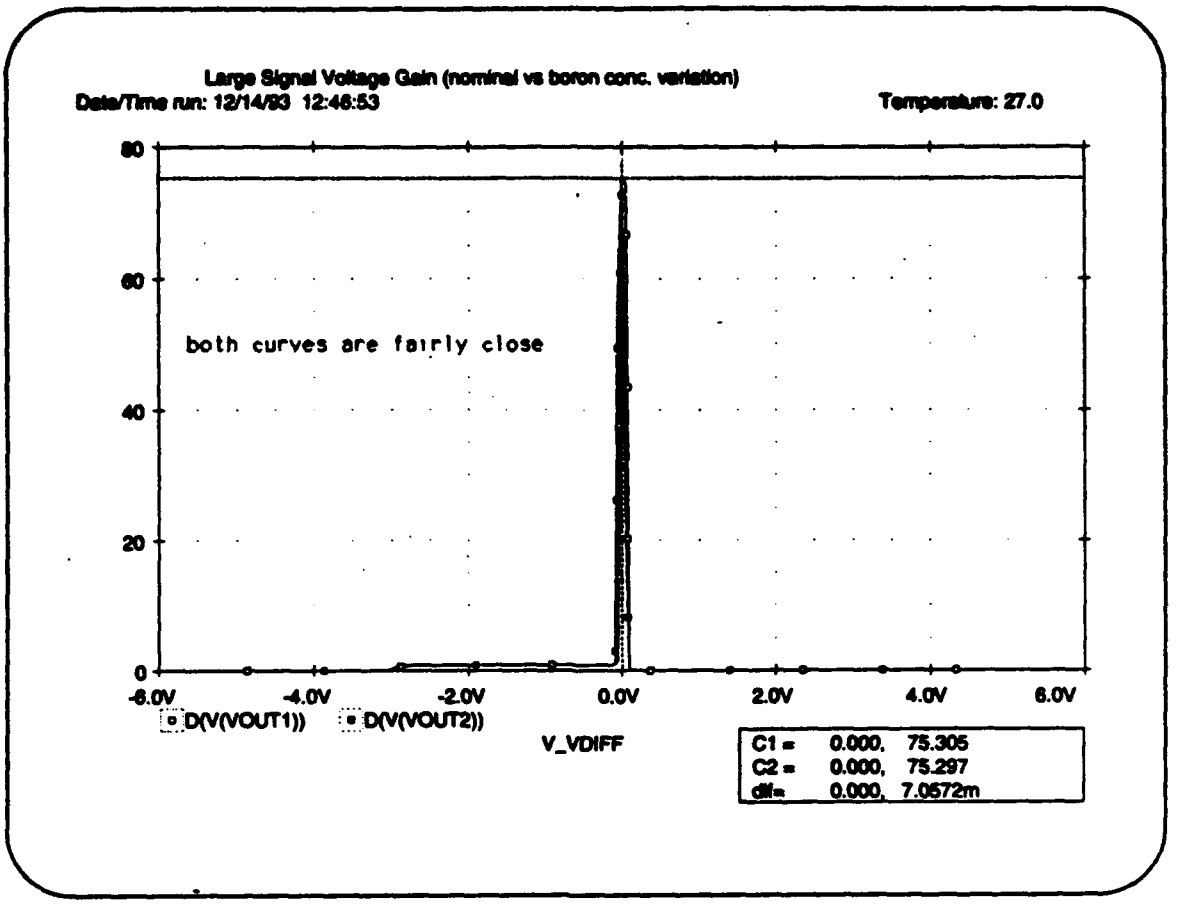

Figure 33. Boron Concentration Process Variation Effect on Large Signal Voltage Gain (Derivative)

From Figure 33 we note a **0.01%** drop in the maximum voltage gain from the nominal value of 75.305 V/V to 75.297 V/V. The power supply current drain characterization for the voltage gain simulation is found in Figure 34.

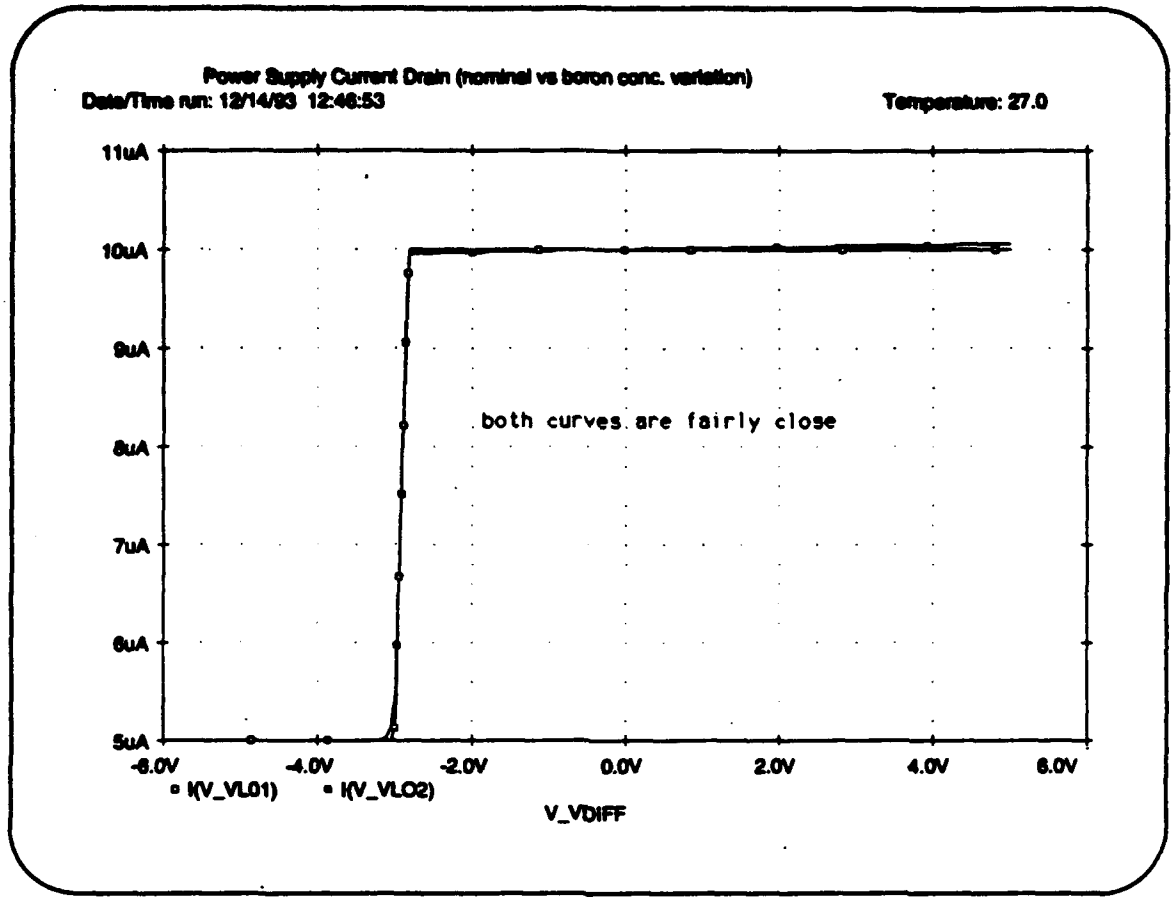

Figure 34. Boron Concentration Variation Effect on Power Supply Current Drain

From this graph we see very little difference in the nominal and varied curves.

The fourth process variation involved a ten percent change in the metal thickness deposition rate from 0.30 microns/min to 0.33 microns/min. This changed the metallization thickness from 0.3 microns to 0.33 microns. The resulting transconductance characterization is found in Figures 35 and 36.

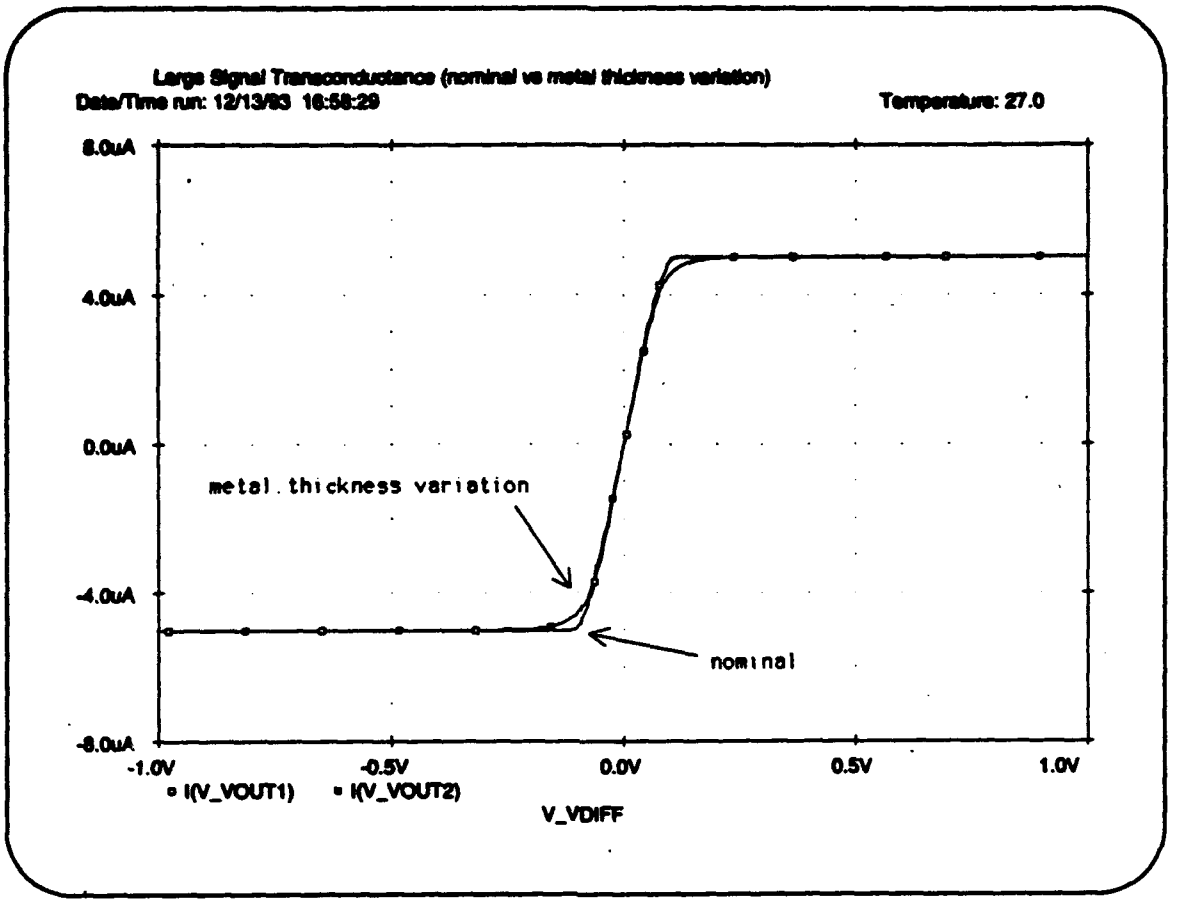

Figure 35. Metal Thickness Process Variation Effect on Large Signal Transconductance

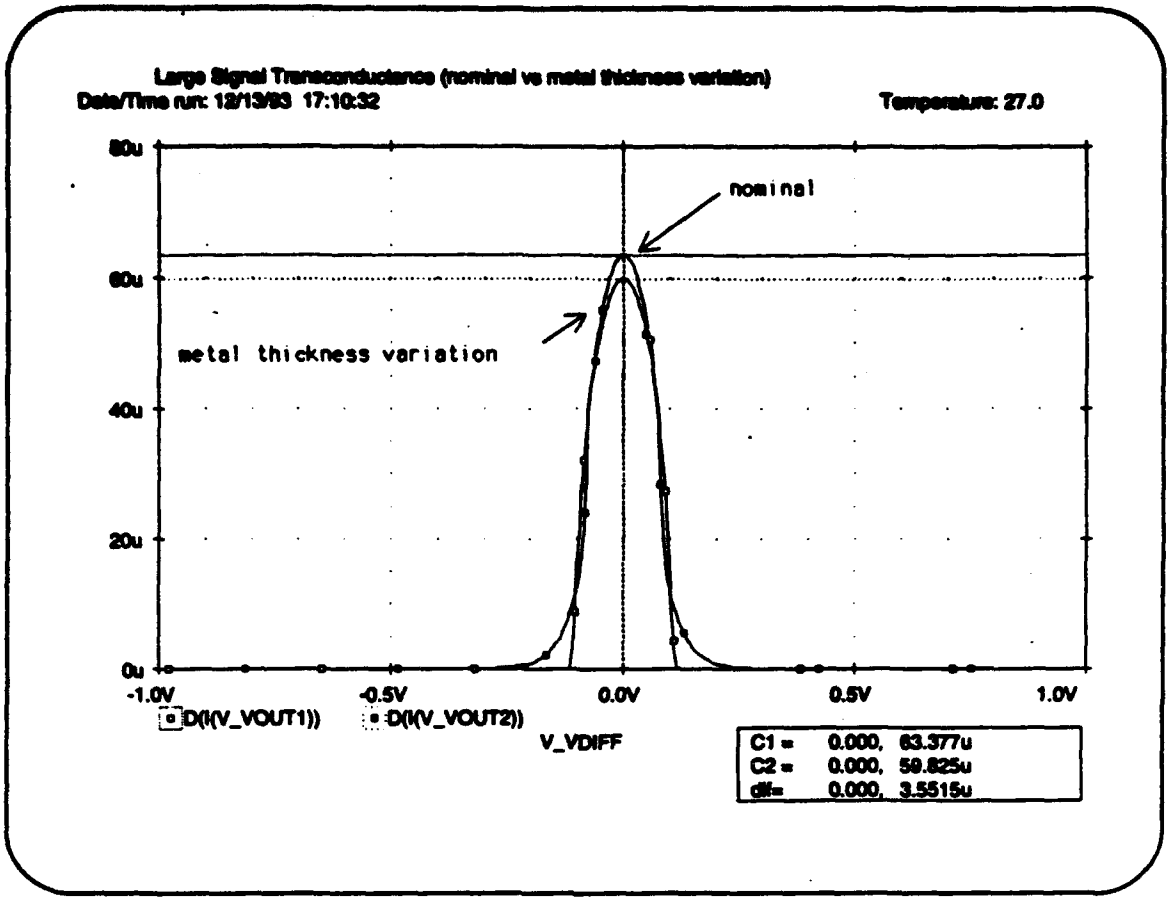

Figure 36. Metal Thickness Process Variation Effect on Large Signal Transconductance (Derivative)

From Figure 36 we note a **5.60%** drop in the maximum transconductance from the nominal value of 63.377 microSiemens to 59.825 microSiemens. The voltage gain characterization is found in Figures 37 and 38.

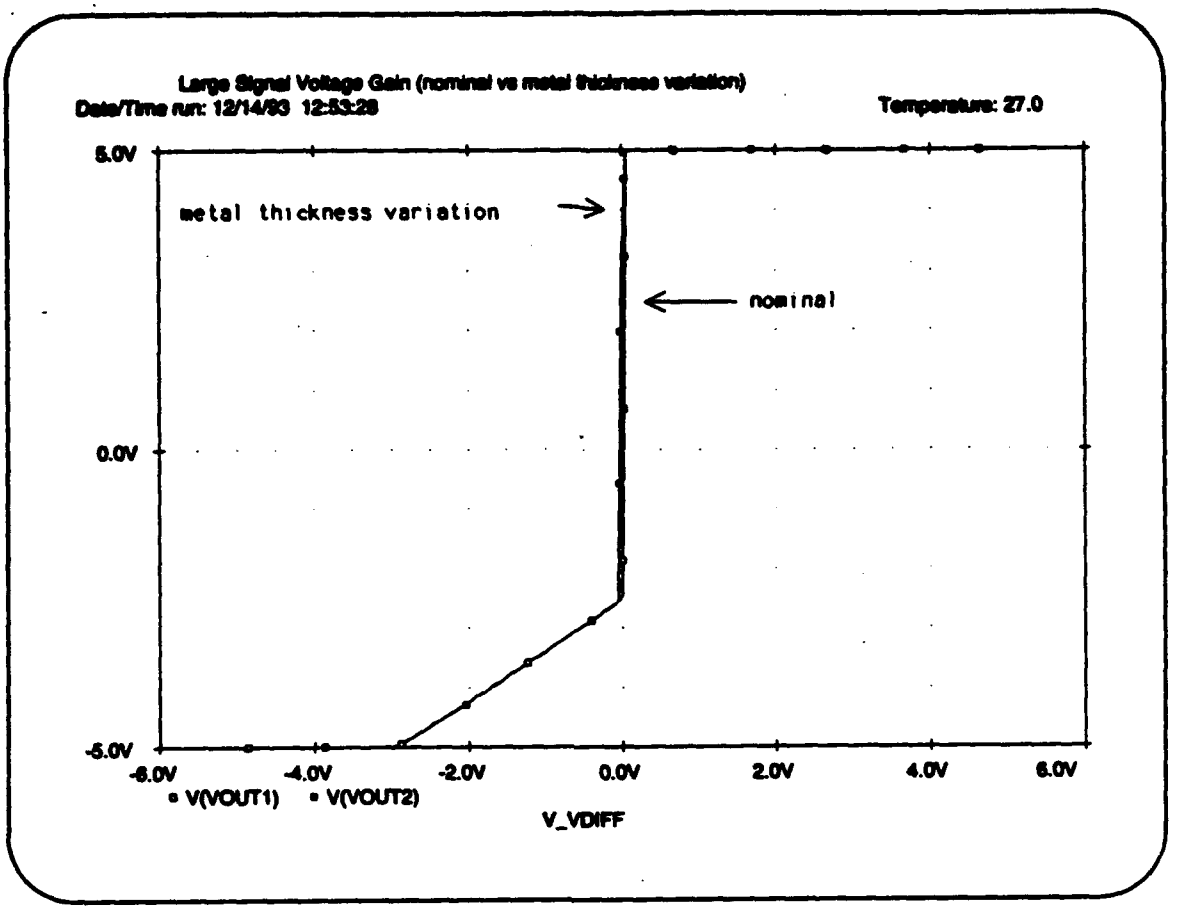

Figure 37. Metal Thickness Process Variation Effect on Large Signal Voltage Gain

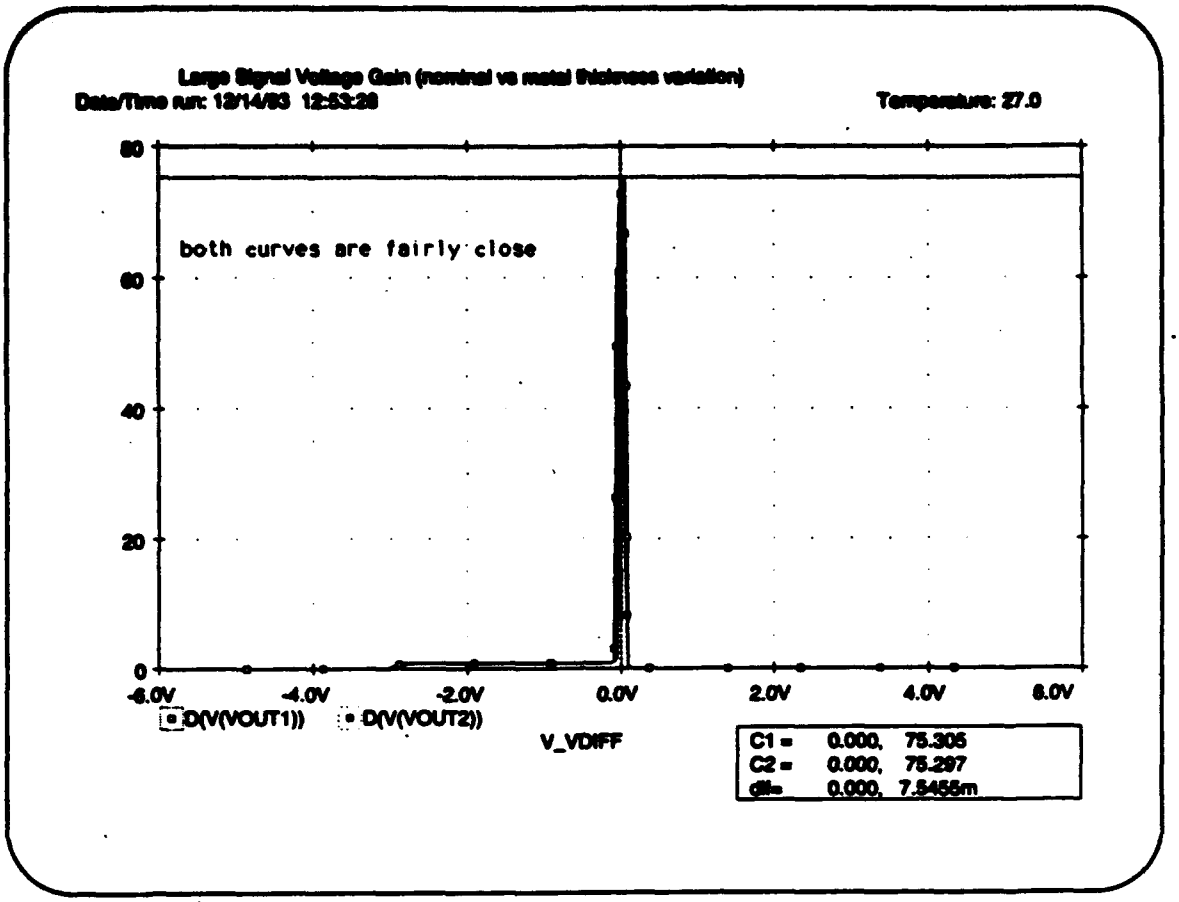

Figure 38. Metal Thickness Process Variation Effect on Large Signal Voltage Gain (Derivative)

From Figure 38 we note a **0.01%** drop in the maximum voltage gain from the nominal value of 75.305 V/V to 75.297 V/V. The power supply current drain characterization for the voltage gain simulation is found in Figure 39.

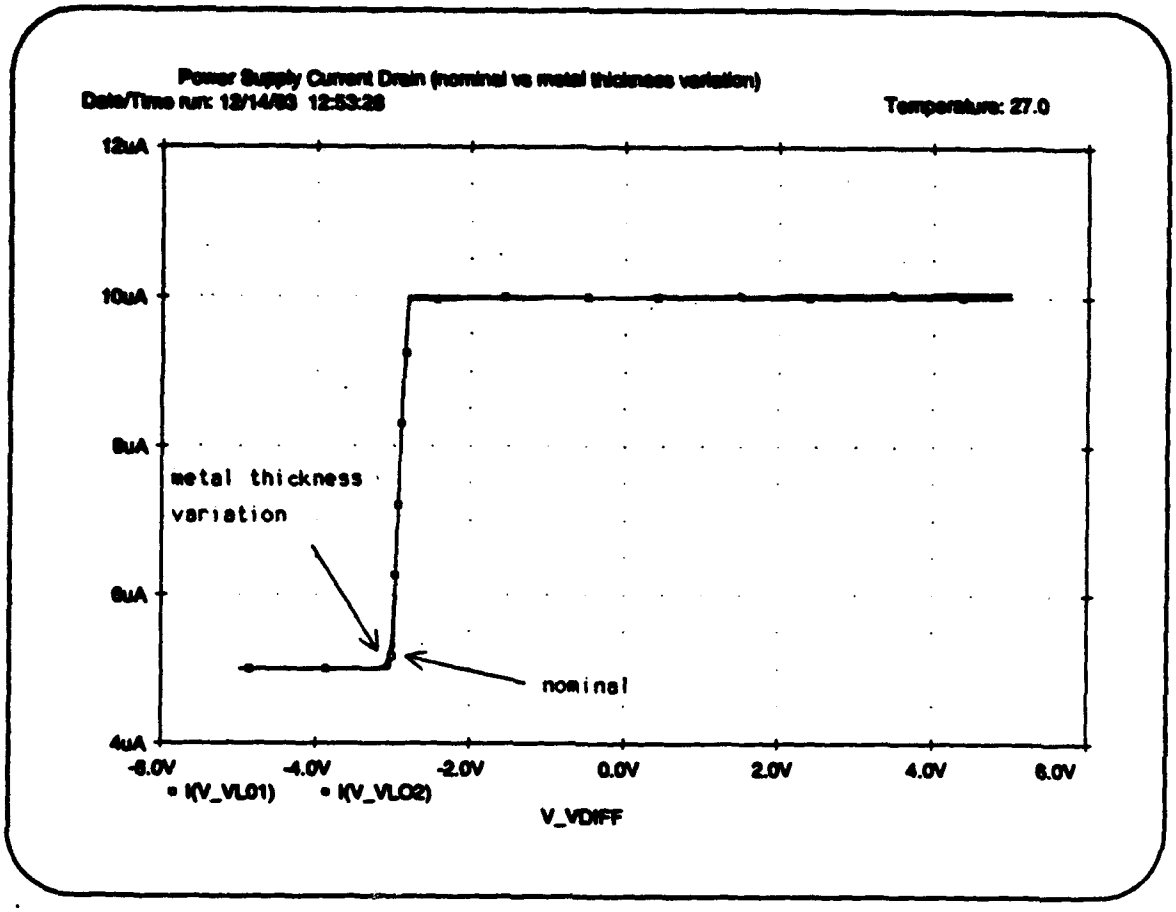

Figure 39. Metal Thickness Variation Effect on Power Supply Current Drain

From this graph we see very little difference in the nominal and varied curves.

The fifth process variation involved a ten percent change in the temperature during the metal deposition from 900 degrees C to 990 degrees C. The resulting transconductance characterization is found in Figures 40 and 41.

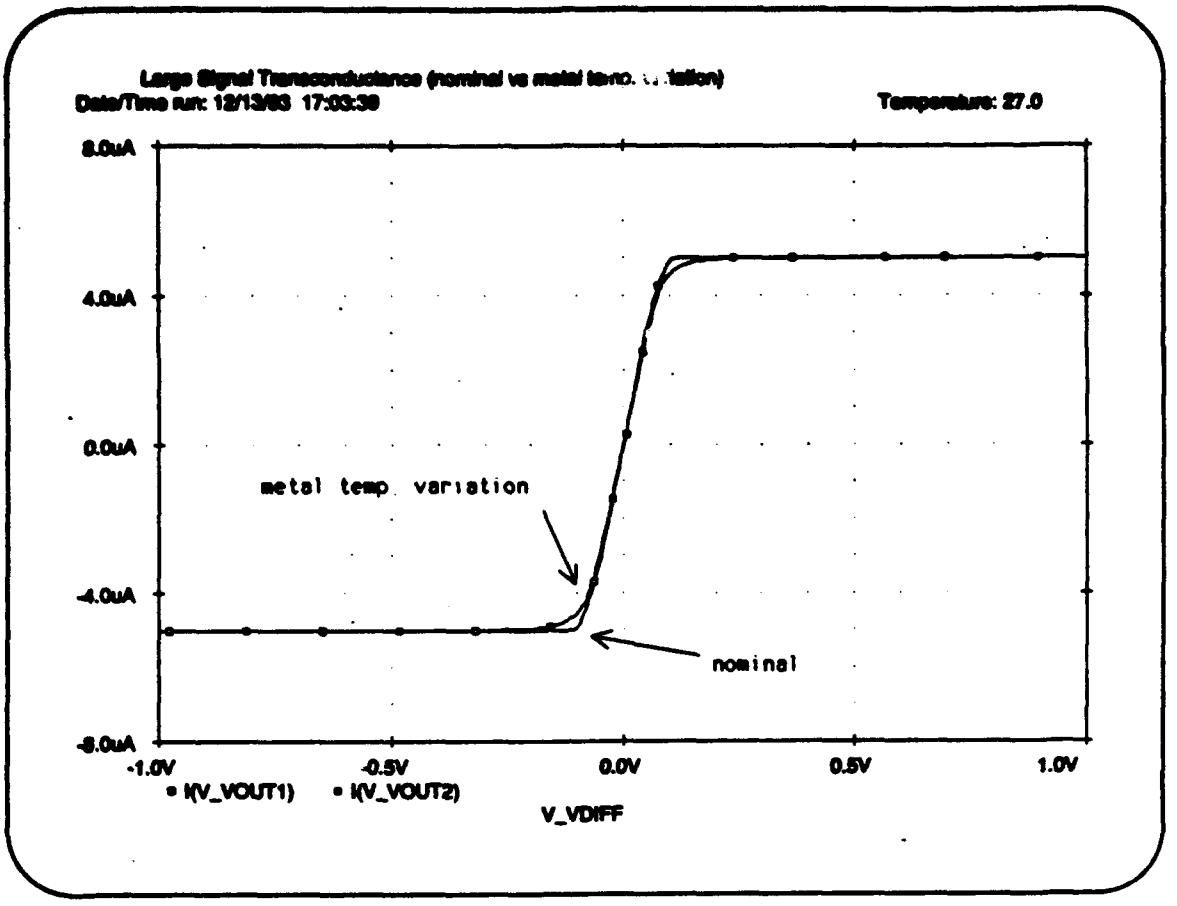

Figure 40. Metal Temperature Process Variation Effect on Large Signal Transconductance

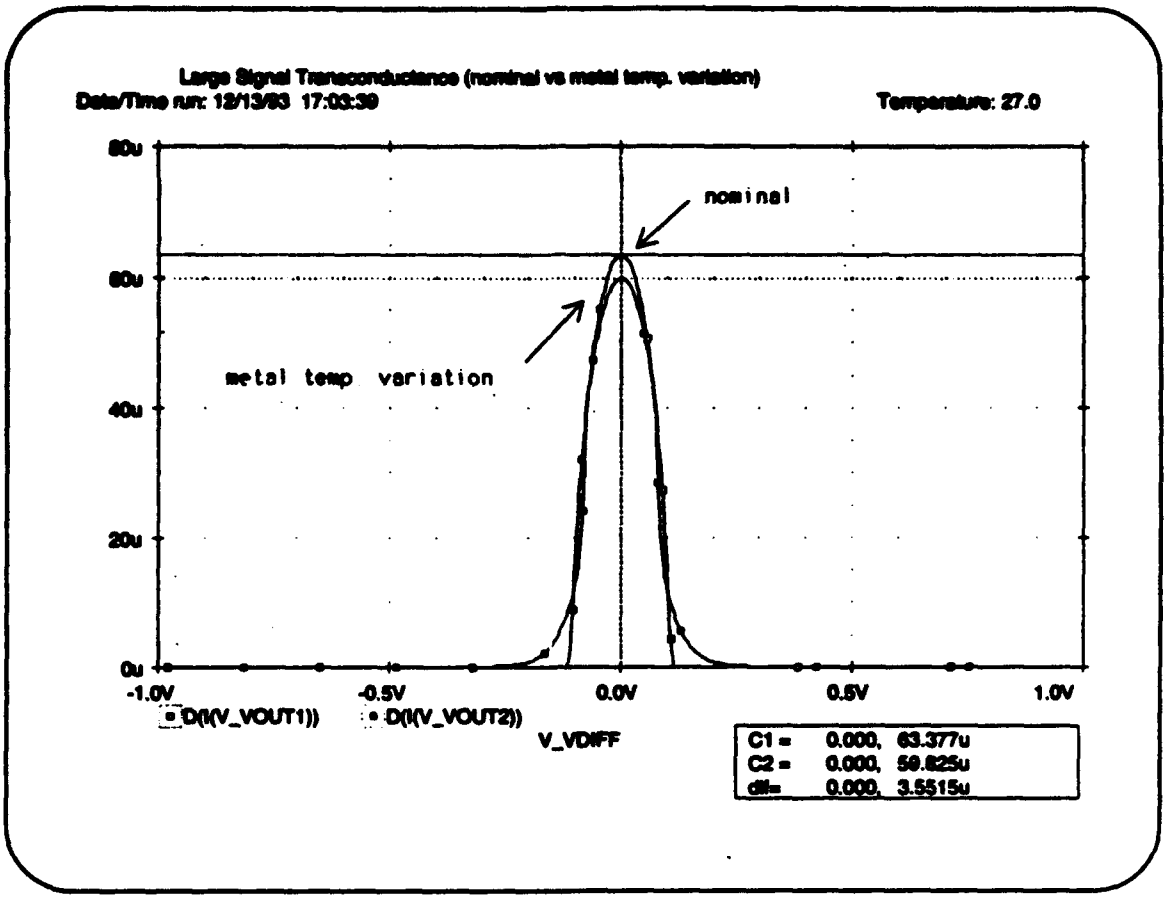

Figure 41. Metal Temperature Process Variation Effect on Large Signal Transconductance (Derivative)

From Figure 41 we note a **5.60%** drop in the maximum transconductance from the nominal value of 63.377 microSiemens to 59.825 microSiemens. The voltage gain characterization is found in Figures 42 and 43.

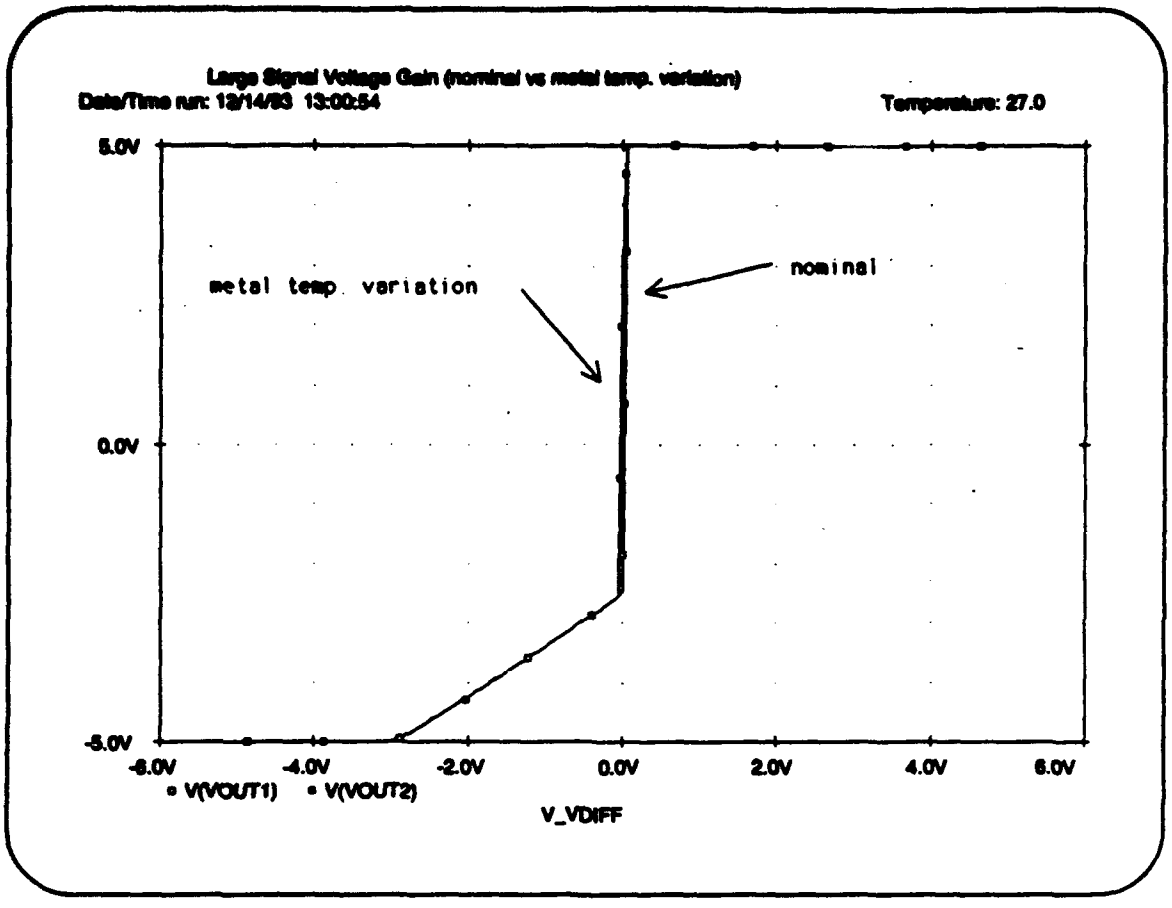

Figure 42. Metal Temperature Process Variation Effect on Large Signal Voltage Gain

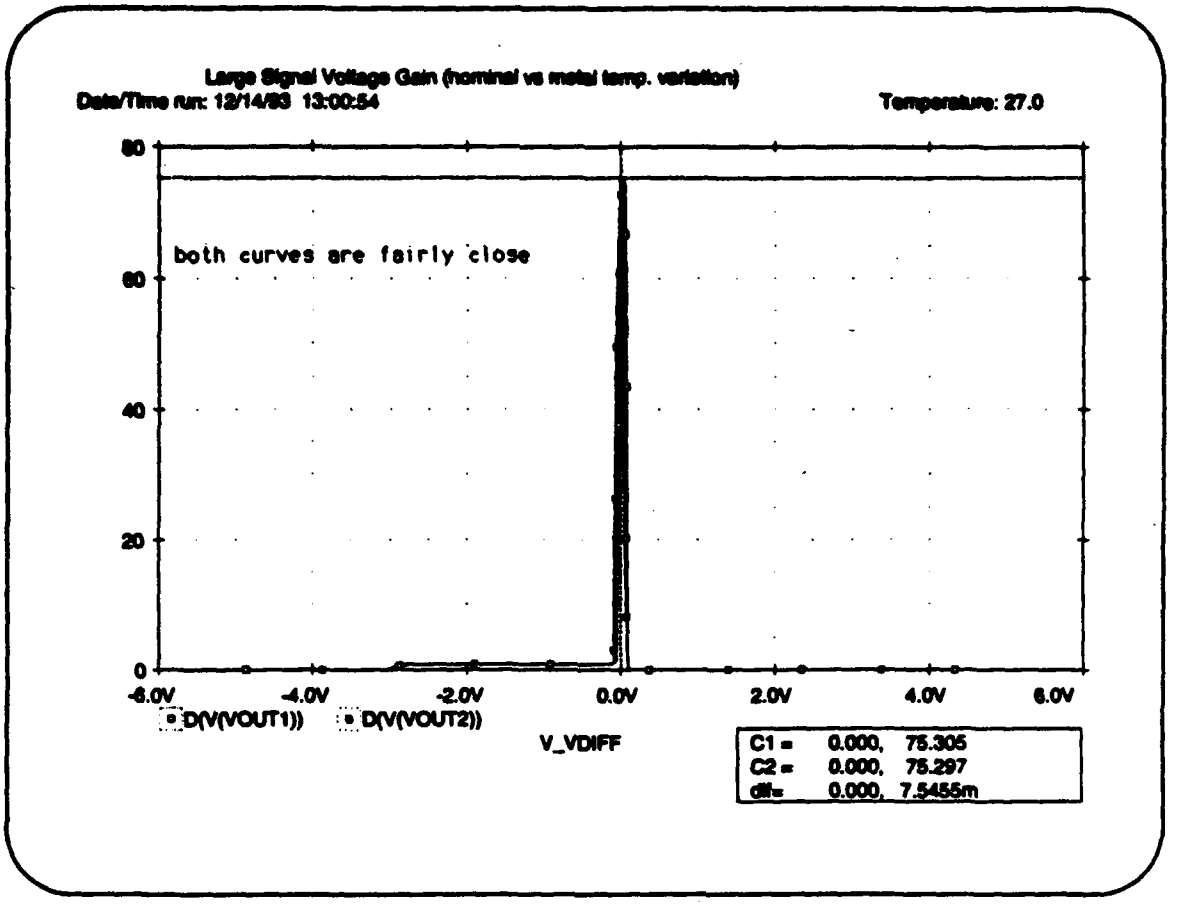

Figure 43. Metal Temperature Process Variation Effect on Large Signal Voltage Gain (Derivative)

From Figure 43 we note a **0.01%** drop in the maximum voltage gain from the nominal value of 75.305 V/V to 75.297 V/V. The power supply current drain characterization for the voltage gain simulation is found in Figure 44.

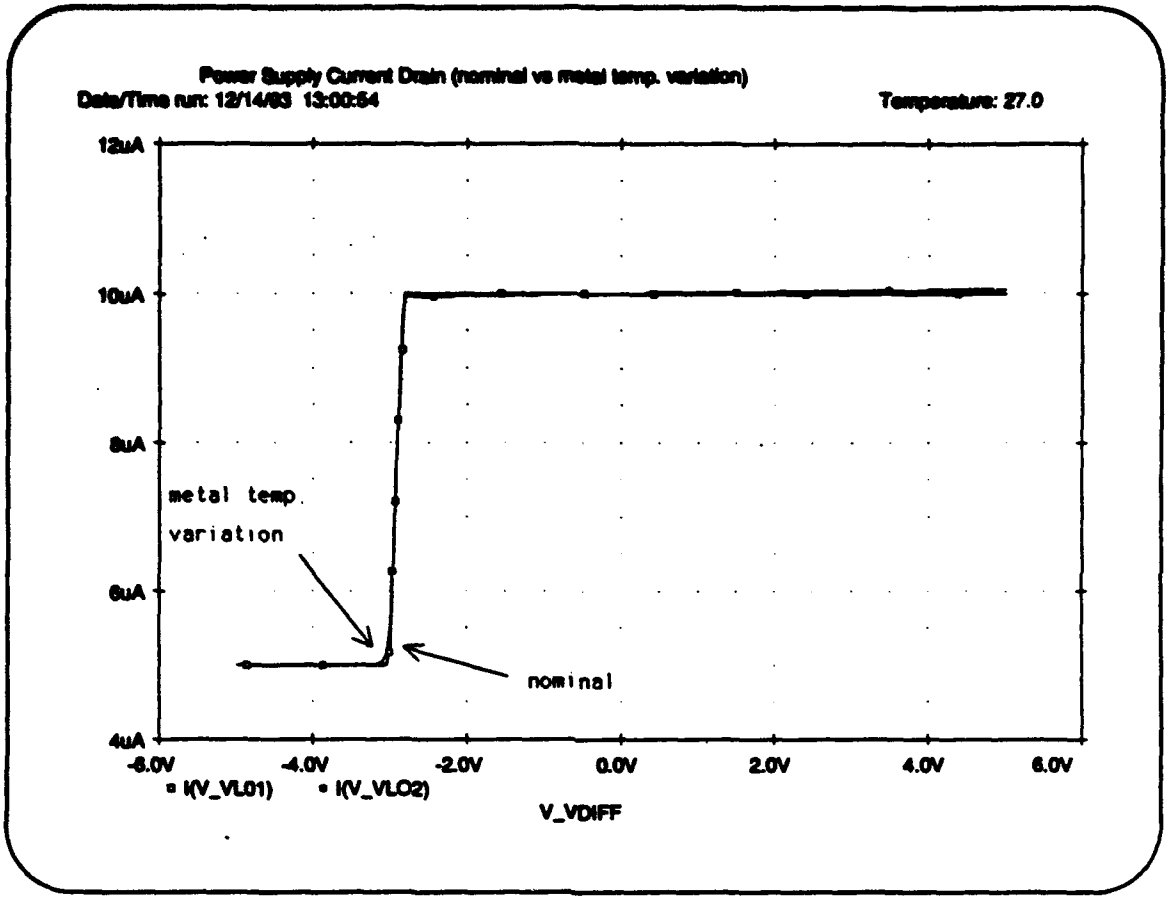

Figure 44. Metal Temperature Variation Effect on Power Supply Current Drain

From this graph we see very little difference in the nominal and varied curves.

The sixth process variation involved a ten percent change in the gate oxide charge density (Qss) from -5.025 cm-2 to -4.5225 cm-2. The resulting transconductance characterization is found in Figures 45 and 46.

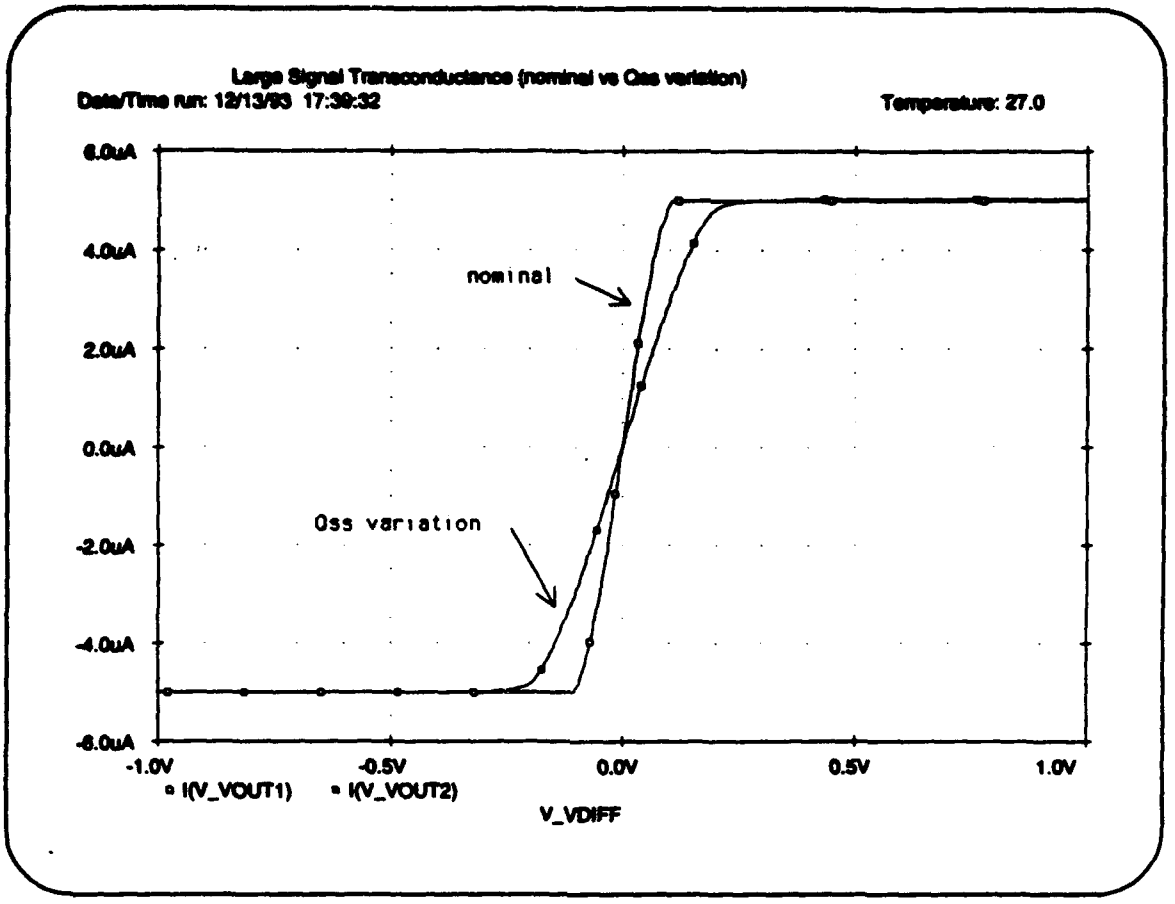

Figure 45. Qss Process Variation Effect on Large Signal Transconductance

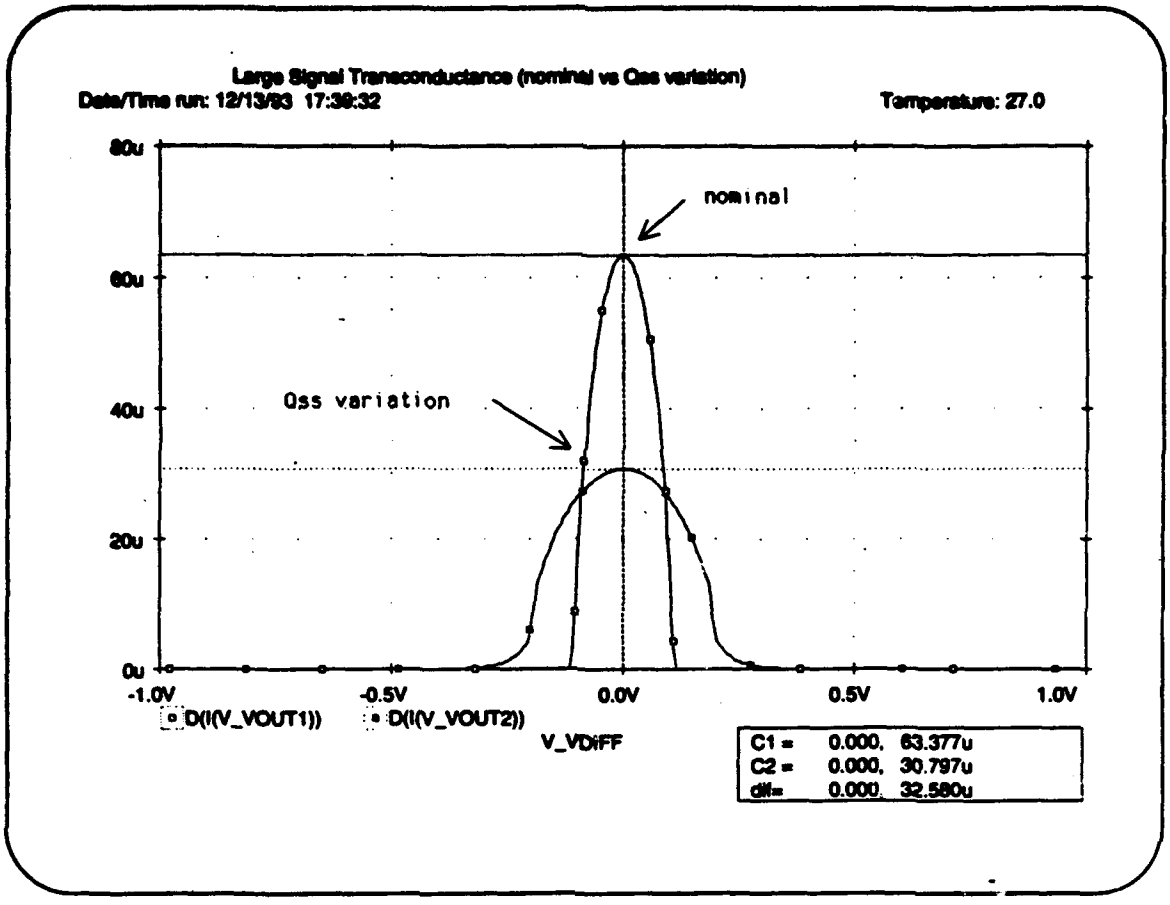

Figure 46. Qss Process Variation Effect on Large Signal Transconductance (Derivative)

From Figure 46 we note a **51.4%** drop in the maximum transconductance from the nominal value of 63.377 microSiemens to 30.797 microSiemens. The voltage gain characterization is found in Figures 47 and 48.

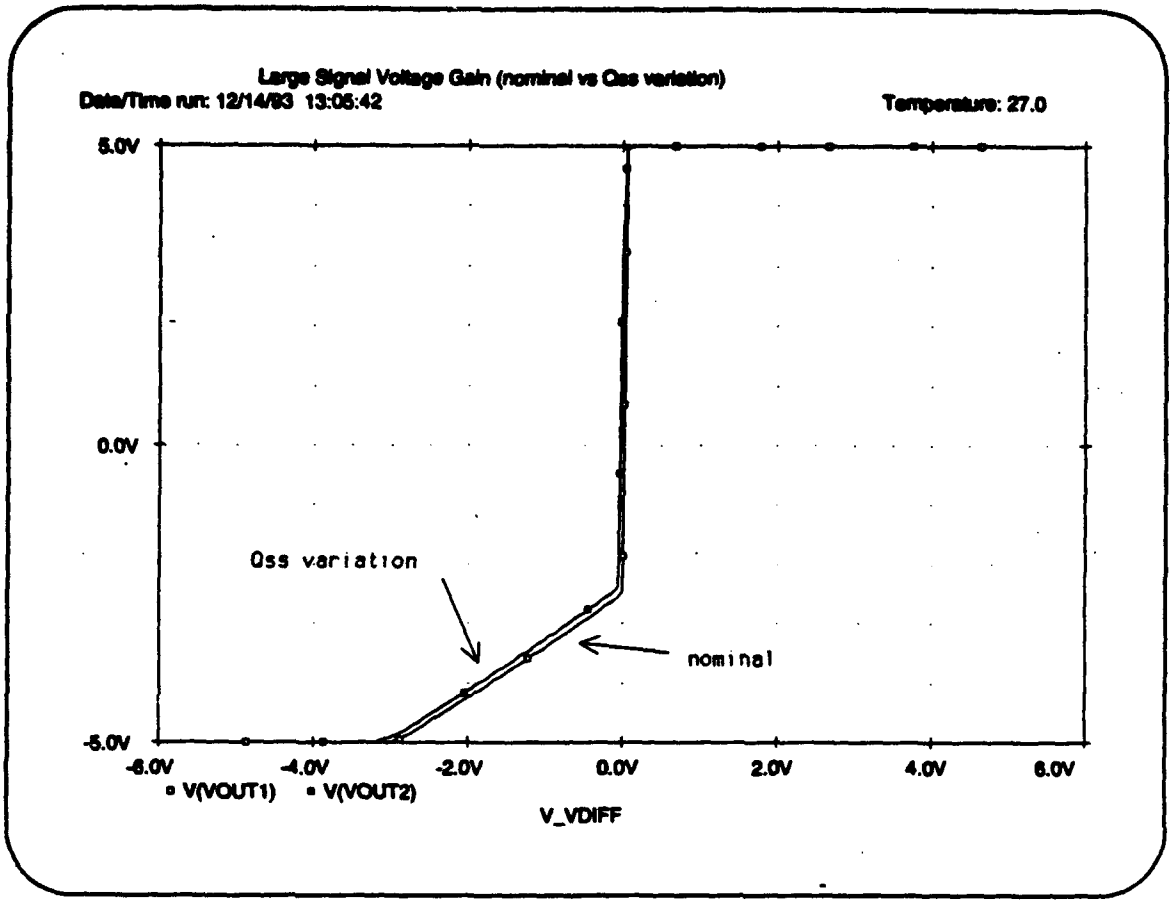

Figure 47. Qss Process Variation Effect on Large Signal Voltage Gain

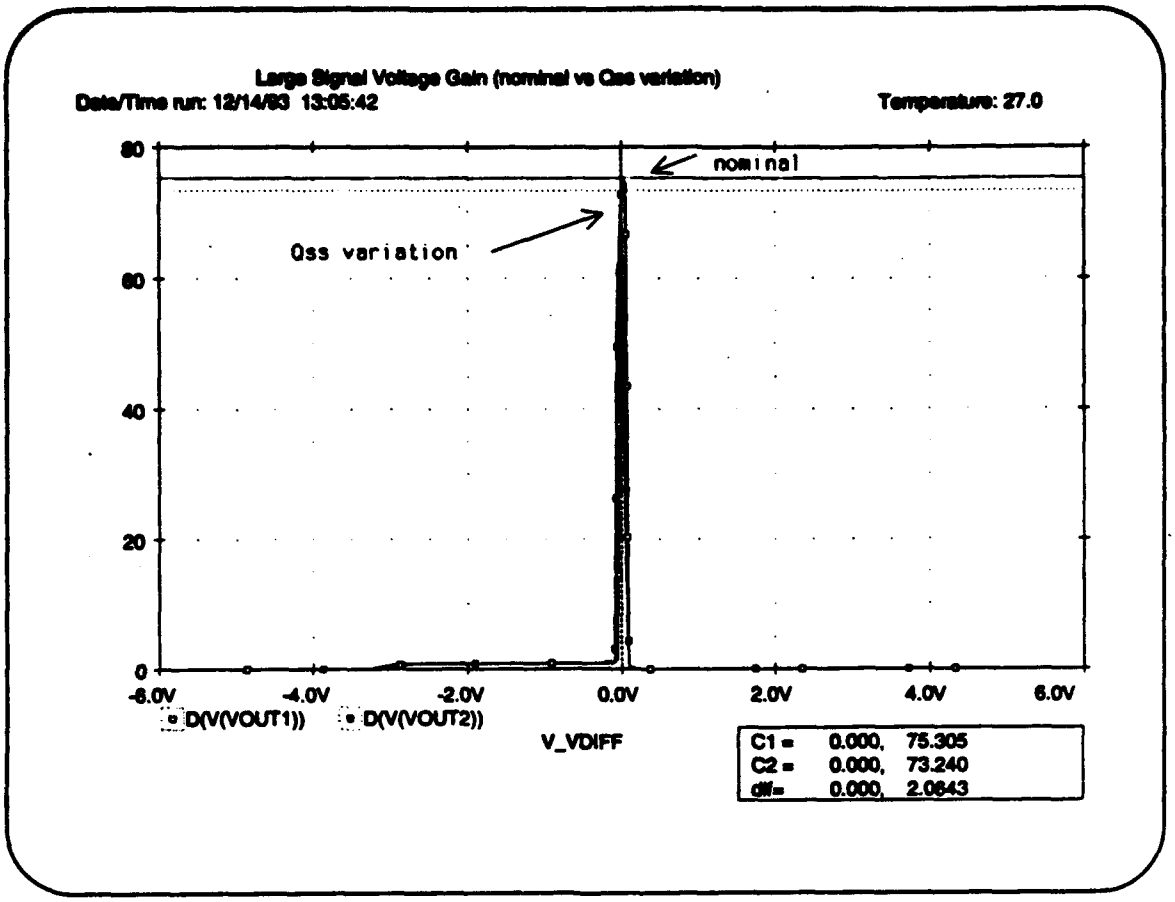

Figure 48. Qss Process Variation Effect on Large Signal Voltage Gain (Derivative)

From Figure 48 we note a **2.74%** drop in the maximum voltage gain from the nominal value of 75.305 V/V to 73.240 V/V. The power supply current drain characterization for the voltage gain simulation is found in Figure 49.

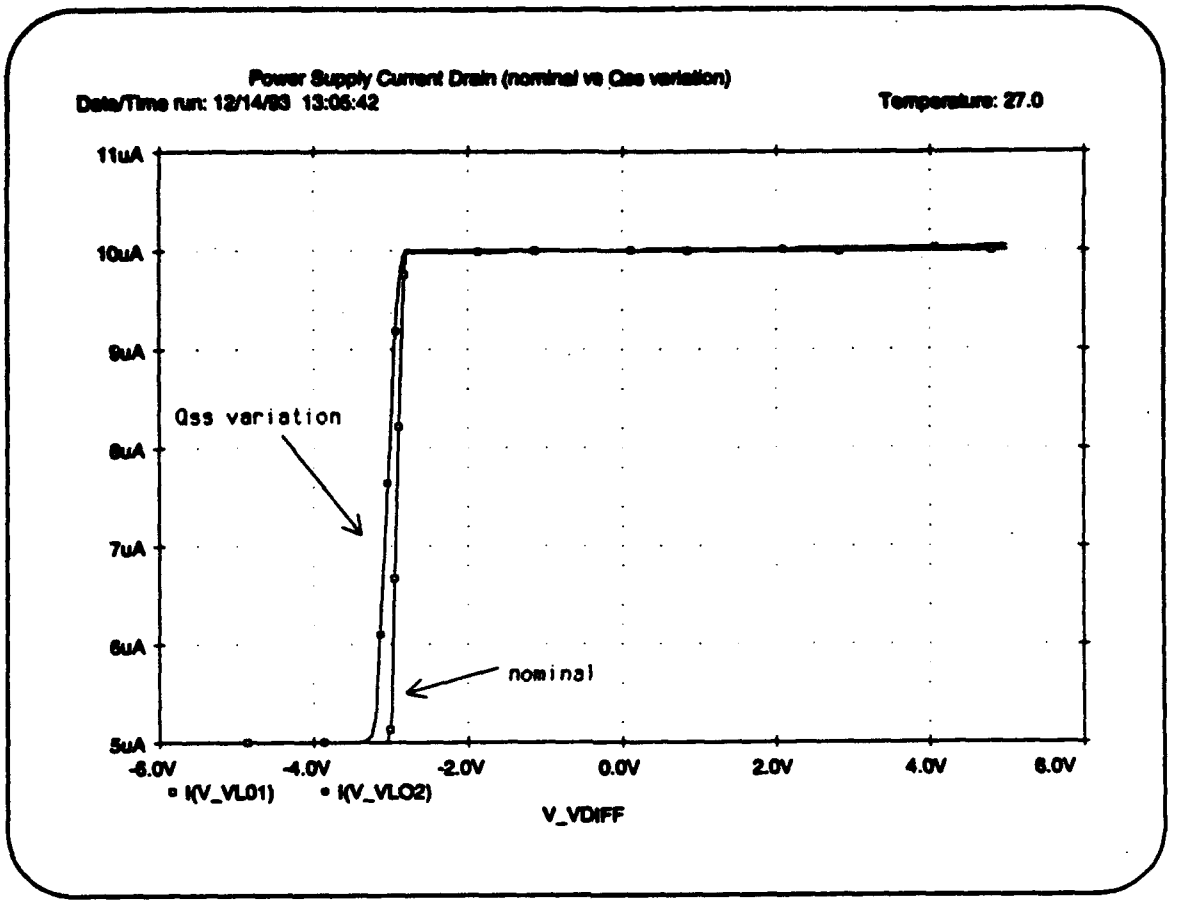

Figure 49. Qss Process Variation Effect on Power Supply Current Drain

From this graph we see only a slight difference in the nominal and varied curves.

(6) For the six process failures, the percent deviation of the two performance characteristics from the nominal were calculated. For this calculation, simulation plot data was used to determine the maximum variation in circuit performance. The results are summarized in Table 2.

Table 2. Performance Variations Resulting From a Two Standard Deviation Increase in Various Process Parameters - GT PMOS Process

Process Parameter (X)	Transconductance (G)	Voltage Gain (H)
X_1, Qss (gate oxide charge density)	51.4%	2.74%
X_2, Gox temperature	-21.4%	16.0%
X_3, Metal temperature	-5.60%	-0.01%
X_4, Metal thickness	-5.60%	-0.01%
X_5, Boron concentration	5.52%	0.01%
X_6, Boron temperature	1.45%	0.01%

(7) Because the application of the microcircuit was not known, a **5 %** deviation was arbitrarily chosen to represent the minimum percent deviation from the norm that constitutes an error for either performance characteristic. Given this standard, a transconductance error was caused by all of the six process failures except the boron predeposition temperature variation. Only the gate oxide growth temperature variation caused an error in voltage gain.

(8) Assuming a normal Gaussian distribution of failures, each failure will have an equal probability of occurrence of **4.56%**. The following equations summarize the calculations made to determine the probability of occurrence for the two errors in circuit performance.

$P = 6, C = 2$

Failures:

X_1 = Qss
X_2 = Gox
X_3 = Tmetal
X_4 = thmetal
X_5 = Nboron
X_6 = Tboron

N = no failures
V = any failure

Probability of 2 standard deviation variation occurring:

$$P\{X_1\} = P\{X_2\} = P\{X_3\} = P\{X_4\} = P\{X_5\} = P\{X_6\} = \mathbf{0.0456}$$

$$P\{\overline{X}_1\} = 1 - 0.0456 = 0.9544$$

$$P\{N\} = P\{\overline{X}_1 \& \overline{X}_2 \& \overline{X}_3 \& \overline{X}_4 \& \overline{X}_5 \& \overline{X}_6\} = P\{\overline{X}_1\} x P\{\overline{X}_2\} x \bullet \bullet \bullet x P\{\overline{X}_6\} = (0.9544)^6 = 0.7558$$

Probability of any one failure occurring:

$$P\{V\} = 1 - P\{N\} = \mathbf{0.2442}$$

Two possible errors assumed (C = 2):

$$G = \Delta g_m > \mathbf{5\ \%}$$
$$H = \Delta A_v > \mathbf{5\ \%}$$

The probability of an error given a specific failure occurs (from simulated data):

G:

$$P\{G|X_1\} = P\{G|X_2\} = P\{G|X_3\} = P\{G|X_4\} = P\{G|X_5\} = 1$$

$$P\{G|X_6\} = 0$$

H:

$$P\{H|X_2\} = 1$$

$$P\{H|X_1\} = P\{H|X_3\} = P\{H|X_4\} = P\{H|X_5\} = P\{H|X_6\} = 0$$

The probability of G given at least one failure occurs:

$$P\{G|V\} = 5/6 = \mathbf{0.833}$$

The probability of H given at least one failure occurs:

$$P\{H|V\} = 1/6 = \mathbf{0.167}$$

The probability of G:

$$P\{G\} = P\{G|V\} \times P\{V\} = (0.833)(0.2442) = 0.2035 = \mathbf{20.35\%}$$

The probability of H:

$$P\{H\} = P\{H|V\} \times P\{V\} = (0.167)(0.2442) = 0.04071 = \mathbf{4.071\%}$$

3.10 Conclusions

A generic methodology has been developed that starts with a process characterization and produces a fault set ranked by probability of occurrence for a particular microcircuit. The methodology utilizes process and circuit simulation tools to map microelectronic process failures to circuit performance. Using statistical and probabilistic data manipulation techniques, circuit performance is translated into a set of possible microcircuit errors ranked by probability of occurrence. These microcircuit errors constitute faults for higher level circuits. The fault set will subsequently be used in fault simulations for circuits at a higher level of integration.

As summarized in the previous results section, this methodology has been demonstrated using the GT PMOS process. For this particular process, variations in Qss and Gox temperature were found to have the most significant effect on circuit performance. Statistical calculations led to the ranking of the two possible circuit performance errors. The probability of a large signal transconductance error occurring is found to be **20.35%**, while the probability of a large signal voltage gain error occurring is found to be **4.071%**. These results constitute the probability ordered fault set for the differential amplifier microcircuit examined in this report.

There are several steps in the methodology that could benefit from computer automation. Although it is probably unlikely that the process tuning can be automated, the process simulations would greatly benefit from automation. Because the computer code for the PREDITOR process simulator is available in the public domain, it is feasible to incorporate changes in the program that allow several simulations to be performed during a single execution. The transfer of data from the process simulator to the circuit simulation program is another candidate for automation. In addition, the results of the circuit simulation could automatically produce a fault set ordered by probability of occurrence. The programming necessary to accomplish all of this could be a major part of future research leading to a more effective implementation of the methodology.

3.11 Acknowledgment

The authors wish to thank Dr. Martin Brooke and Dr. Gary May for their helpful suggestions. We would also like to thank Dr. Hank Walker for his help in providing us with the PREDITOR simulation software.

Appendix A
SPICE2 Circuit Parameters From MOSIS Process

PMOS Device Data, 5/24/93, L = 2 microns

Device #	Width	VT0	Lambda	KP	Gamma
1	3	0.721975	0.102771	0.0000133	0.500023
2	3	0.722045	0.105127	0.0000135	0.495954
3	3	0.700718	0.10453	0.000013	0.509092
4	3	0.70055	0.106765	0.0000131	0.512216
5	3	0.706008	0.098921	0.0000124	0.517296
6	3	0.709615	0.102099	0.0000126	0.518945
7	3	0.718757	0.094957	0.0000127	0.510938
8	3	0.685715	0.099802	0.0000125	0.518439
9	3	0.63579	0.110384	0.0000139	0.493736
10	3	0.618658	0.103924	0.0000137	0.502172
11	3	0.651205	0.102305	0.0000137	0.503019
12	3	0.703985	0.104615	0.0000139	0.496248
13	3	0.654397	0.105787	0.000014	0.489966
14	3	0.631184	0.117019	0.0000136	0.482015
15	3	0.679593	0.107077	0.0000133	0.485688
16	3	0.657459	0.109354	0.0000132	0.507682
Statistics	Average	0.68110338	0.10471481	1.3275E-05	0.50271431
	Std. Dev.	0.0347549	0.00507395	5.2217E-07	0.0115563
	Variance	0.0012079	2.5745E-05	2.7267E-13	0.00013355

PMOS Device Data, 5/24/93, L = 2 microns

Device #	Width	VT0	Lambda	KP	Gamma
1	6	0.681496	0.106586	0.0000132	0.502606
2	6	0.715167	0.102797	0.0000131	0.504728
3	6	0.711765	0.099804	0.0000127	0.510461
4	6	0.700435	0.103382	0.0000126	0.512549
5	6	0.719596	0.094106	0.0000124	0.519072
6	6	0.662798	0.110332	0.000014	0.489545
7	6	0.671206	0.104658	0.0000139	0.484417
8	6	0.710564	0.101733	0.0000136	0.508056
9	6	0.642973	0.115224	0.0000135	0.494679
10	6	0.654491	0.112688	0.0000135	0.495934
11	6	0.690002	0.108114	0.0000131	0.508247
Statistics	Average	0.687318	0.105402	0.000013	0.502754
	Std. Dev.	0.026596	0.006053	0.000001	0.010518
	Variance	0.000707	0.000037	0.000000	0.000111

PMOS Device Data, 5/24/93, L = 2 microns

Device #	Width	VT0	Lambda	KP	Gamma
1	12	0.66304	0.108178	0.000013	0.512584
2	12	0.733753	0.098023	0.0000123	0.522013

3	12	0.719964	0.097128	0.0000125	0.516418
4	12	0.688478	0.105695	0.0000138	0.501176
5	12	0.672972	0.104759	0.0000138	0.498886
6	12	0.674064	0.109007	0.0000135	0.480741
7	12	0.648019	0.11128	0.0000134	0.485743
Statistics	Average	0.685756	0.104867	0.000013	0.502509
	Std. Dev.	0.030880	0.005426	0.000001	0.015520
	Variance	0.000954	0.000029	0.000000	0.000241

NMOS Device Data, 5/24/93, L = 2 microns

Device #	Width	VT0	Lambda	KN	Gamma
1	3	0.725727	0.05306	3.54E-05	0.540319
2	3	0.725727	0.05306	3.54E-05	0.540319
3	3	0.708451	0.060061	3.50E-05	0.535909
4	3	0.708886	0.05917	3.43E-05	0.565584
5	3	0.725111	0.059751	3.49E-05	0.556141
6	3	0.68715	0.061533	3.60E-05	0.522624
7	3	0.717739	0.06183	3.71E-05	0.519216
8	3	0.691069	0.062563	3.63E-05	0.531649
9	3	0.701742	0.058735	3.58E-05	0.527882
10	3	0.720445	0.058048	3.65E-05	0.536725
11	3	0.709624	0.058088	3.51E-05	0.550044
12	3	0.710614	0.059764	3.49E-05	0.540786
13	3	0.727928	0.058429	3.56E-05	0.574433
14	3	0.716272	0.060257	3.61E-05	0.580309
15	3	0.721898	0.046537	3.72E-05	0.568715
16	3	0.717901	0.059328	3.41E-05	0.544386
17	3	0.718117	0.059821	3.55E-05	0.525769
18	3	0.707989	0.059987	3.53E-05	0.515803
Statistics	Average	0.71346611	0.05833456	3.5583E-05	0.54314517
	Std. Dev.	0.01153839	0.00385636	8.4939E-07	0.0191878
	Variance	0.00013313	1.4871E-05	7.2147E-13	0.00036817

NMOS Device Data, 5/24/93, L = 2 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	6	0.714467	0.059981	3.47E-05	0.53289
2	6	0.714625	0.059574	3.47E-05	0.532947
3	6	0.714467	0.059981	3.47E-05	0.53289
4	6	0.714625	0.059574	3.47E-05	0.532947
5	6	0.7253	0.059599	3.47E-05	0.543636
6	6	0.697609	0.061789	3.61E-05	0.525732
7	6	0.704943	0.060255	3.69E-05	0.542389
8	6	0.713312	0.059426	3.61E-05	0.531034
9	6	0.706968	0.058963	3.50E-05	0.530564
10	6	0.715451	0.058416	3.49E-05	0.539073

11	6	0.741965	0.055946	3.51E-05	0.577053
12	6	0.738786	0.056626	3.58E-05	0.563353
13	6	0.72247	0.057113	3.44E-05	0.561703
14	6	0.714582	0.060581	3.50E-05	0.546974
15	6	0.69843	0.060525	3.44E-05	0.547169
16	6	0.714977	0.058915	3.46E-05	0.533549
Statistics	Average	0.71581106	0.059204	3.5113E-05	0.54211894
	Std. Dev.	0.01208579	0.00153861	7.2192E-07	0.01426534
	Variance	0.00014607	2.3673E-06	5.2117E-13	0.0002035

NMOS Device Data, 5/24/93, L = 2 microns

Device #	Width	VT0	Lambda	KN	Gamma
1	12	0.72266	0.060232	3.43E-05	0.531159
2	12	0.716484	0.059664	3.44E-05	0.545843
3	12	0.716524	0.059781	3.44E-05	0.54591
4	12	0.706676	0.060317	3.58E-05	0.532953
5	12	0.700569	0.061763	3.61E-05	0.52455
6	12	0.712106	0.058455	3.51E-05	0.545765
7	12	0.728788	0.05826	3.58E-05	0.57371
8	12	0.733856	0.055427	3.44E-05	0.558633
9	12	0.720581	0.058584	3.44E-05	0.5365
10	12	0.715704	0.059712	3.46E-05	0.537024
Statistics	Average	7.17E-01	5.92E-02	3.49E-05	5.43E-01
	Std. Dev.	0.00982666	0.00169137	7.1032E-07	0.01441754
	Variance	9.6563E-05	2.8607E-06	5.0456E-13	0.00020787

PMOS Device Data, 5/25/93, L = 10 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	3	1.015014	0.011311	6.22E-05	0.614756
2	3	1.016924	0.007771	6.21E-05	0.614837
3	3	1.014701	0.011466	6.15E-05	0.621465
4	3	1.023695	0.00782	6.22E-05	0.620195
5	3	0.97406	0.012518	6.08E-05	0.610022
6	3	0.995152	0.008391	6.17E-05	0.606236
7	3	1.01359	0.00765	6.30E-05	0.616298
8	3	1.003437	0.011885	6.28E-05	0.624374
9	3	1.041552	0.010822	6.20E-05	0.614981
10	3	1.037392	0.007896	6.22E-05	0.612318
11	3	1.032706	0.011576	6.16E-05	0.616665
12	3	1.031572	0.012364	6.15E-05	0.608961
13	3	1.040206	0.007896	6.26E-05	0.619222
14	3	1.041158	0.012364	6.24E-05	0.613945
15	3	1.043725	0.007967	6.20E-05	0.610688
16	3	1.039847	0.00718	6.18E-05	0.614904
Statistics	Average	1.02279569	0.00980481	6.2025E-05	0.61499169
	Std. Dev.	0.01978109	0.00210174	5.4833E-07	0.00478881

Variance	0.00039129	4.4173E-06	3.0067E-13	2.2933E-05

PMOS Device Data, 5/25/93, L = 10 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	6	1.011078	0.008752	6.22E-05	0.623956
2	6	1.015606	0.008814	6.17E-05	0.611596
3	6	0.98936	0.008648	6.10E-05	0.575892
4	6	1.009487	0.008631	6.29E-05	0.622752
5	6	1.007409	0.008631	6.28E-05	0.619923
6	6	1.034875	0.007123	6.21E-05	0.614845
7	6	1.039709	0.00895	6.22E-05	0.616916
8	6	1.03162	0.007163	6.15E-05	0.602457
9	6	1.040237	0.009033	6.15E-05	0.614402
10	6	1.042268	0.009014	6.18E-05	0.612537
11	6	1.039811	0.009014	6.18E-05	0.618601
Statistics	Average	1.023769	0.008525	0.000062	0.612171
	Std. Dev.	0.017869	0.000701	0.000001	0.013409
	Variance	0.000319	0.000000	0.000000	0.000180

PMOS Device Data, 5/25/93, L = 10 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	12	1.012564	0.009777	6.21E-05	0.620417
2	12	1.012502	0.007917	6.15E-05	0.624306
3	12	1.001139	0.010574	6.19E-05	0.606509
4	12	1.006966	0.008602	6.28E-05	0.618012
5	12	1.03966	0.008094	6.17E-05	0.613681
6	12	1.031266	0.008881	6.22E-05	0.615458
7	12	1.037534	0.009	6.15E-05	0.61608
8	12	1.039878	0.010945	6.21E-05	0.609635
Statistics	Average	1.022689	0.009224	0.000062	0.615512
	Std. Dev.	0.016015	0.001110	0.000000	0.005694
	Variance	0.000256	0.000001	0.000000	0.000032

NMOS Device Data, 4/25/93, L = 10 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	3	0.831531	0.009567	3.35E-05	0.67691
2	3	0.834061	0.009876	3.39E-05	0.674056
3	3	0.833302	0.009955	3.37E-05	6.80E-01
4	3	0.833767	0.010514	3.34E-05	0.692005
5	3	0.827288	0.009578	3.30E-05	0.687725
6	3	0.82534	0.010019	3.34E-05	0.684031
7	3	0.825714	0.009664	3.29E-05	0.688741
8	3	0.829049	0.009445	3.32E-05	0.684918
9	3	0.832492	0.009978	3.38E-05	0.683906
10	3	0.833093	0.009164	3.41E-05	0.683301

11	3	0.834247	0.009892	3.41E-05	0.690436
12	3	0.835017	0.009431	3.37E-05	0.683349
13	3	0.812973	0.009996	3.63E-05	0.686915
14	3	0.815665	0.009731	3.68E-05	0.682066
15	3	0.81416	0.010196	3.66E-05	0.68475
16	3	0.810704	0.009909	3.64E-05	0.686905
Statistics Average		0.82677519	0.00980719	0.0000343	0.68437938
Std. Dev.		0.00857718	0.00032939	1.3731E-06	0.00467092
Variance		7.3568E-05	1.085E-07	1.8853E-12	2.1817E-05

NMOS Device Data, 4/25/93, L = 10 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	6	0.830592	0.009442	3.37E-05	0.68515
2	6	0.829095	0.009775	3.36E-05	0.677961
3	6	0.835976	0.00987	3.34E-05	0.678164
4	6	0.827031	0.00975	3.32E-05	0.683913
5	6	0.822569	0.010409	3.33E-05	0.685875
6	6	0.827946	0.01022	3.28E-05	0.687218
7	6	0.834447	0.00994	3.39E-05	0.683239
8	6	0.83395	0.009564	3.41E-05	0.681944
9	6	0.834832	0.009835	3.38E-05	0.686396
10	6	0.815366	0.010169	3.65E-05	0.681942
11	6	0.813108	0.010386	3.65E-05	0.67921
12	6	0.814081	0.010232	3.65E-05	0.679265
Statistics Average		0.82658275	0.009966	3.4275E-05	0.68252308
Std. Dev.		0.00840259	0.00031558	1.3844E-06	0.00329877
Variance		7.0604E-05	9.9591E-08	1.9166E-12	1.0882E-05

NMOS Device Data, 4/25/93, L = 10 microns

Device #	Width	VTO	Lambda	KN	Gamma
1	12	0.832139	0.010093	3.38E-05	0.682729
2	12	0.831489	0.009628	3.29E-05	0.68859
3	12	0.827776	0.0098	3.31E-05	0.684158
4	12	0.835313	0.010045	3.37E-05	0.684438
5	12	0.832215	0.010036	3.41E-05	0.678783
6	12	0.814349	0.010139	3.62E-05	0.683706
7	12	0.814266	0.009965	3.66E-05	0.681335
Statistics Average		8.27E-01	9.96E-03	3.43E-05	6.83E-01
Std. Dev.		0.00880687	0.00018191	1.4684E-06	0.00301972
Variance		7.7561E-05	3.3092E-08	2.1562E-12	9.1187E-06

Appendix B
Details of Georgia Tech PMOS Process

GT PMOS Process Steps Specified For PREDITOR
November 12, 1993

1.SUBSTRATE step	
step name (string)	Substrate
Impurity	PHOSPHORUS
Doping	2.3e+15
Thickness	0.15
2.INITIALIZE step	
SAMPLE_STAT	0
Reread_File	1
RNG_FILE_NAME	picrngchip.dat
3.OXIDIZE step	
step name (string)	Grow_Oxide_Dry
Type	DRY
Time	15
Temp	1100
Ramping Rate	0
Rho-O2	0.5
Rho-HCl	0
VAR:Time	0
VAR:Temp	0
VAR:Rho-O2	0
VAR:Rho-HCl	0
4.OXIDIZE step	
step name (string)	Grow_Oxide_Wet
Type	WET
Time	60
Temp	1100
Ramping Rate	0
Rho-O2	0.99
Rho-HCl	0
VAR:Time	0
VAR:Temp	0
VAR:Rho-O2	0
VAR:Rho-HCl	0
5.OXIDIZE step	
step name (string)	Grow_Oxide_Dry

Type	DRY
Time	15
Temp	1100
Ramping Rate	0
Rho-O2	0.5
Rho-HCl	0
VAR:Time	0
VAR:Temp	0
VAR:Rho-O2	0
VAR:Rho-HCl	0

6.INLINE step	
step name (string)	IL_fld_ox
Location	<453.06628 828.535645>
Thickness	yes
Resistivity	no
Si_Junction	no
Si_SheetResistance	no

7.PHOTOLITH step	
step name (string)	PhotolithS/D
Wavelength	4358A
Type	1_to_1
Dose	150
Distance	6
Resist_Thickness	1
Time	25
Sign	POSITIVE
Mask_Name	S/D
VAR:Dose	0
VAR:Distance	0
VAR:Resist	0
VAR:Time	0

8.ETCH step	
step name (string)	Define_Source/Drain
Material	OXIDE
Time	1
Rate	0.66 (um/min)
VAR:Time	0
VAR:Rate	0

9.ETCH step	
step name (string)	Photoresist_removal
Material	RESIST

Time	1
Rate	1 (um/min)
VAR:Time	0
VAR:Rate	0

10.DIFFUSE step

step name (string)	Boron_Predeposition
Impurity	Boron
Time	30
Temp	1100
Dose	1e+19
VAR:Time	0
VAR:Temp	0
VAR:Temp	0

11.PHOTOLITH step

step name (string)	Photolith_Active
Wavelength	4358A
Type	1_to_1
Dose	150
Distance	6
Resist_Thickness	1
Time	10
Sign	NEGATIVE
Mask_Name	ACT
VAR:Dose	0
VAR:Distance	0
VAR:Resist	0
VAR:Time	0

12.ETCH step

step name (string)	Define_Active_Areas
Material	OXIDE
Time	1
Rate	39.6 (um/min)
VAR:Time	0
VAR:Rate	0

13.ETCH step

step name (string)	Photoresist_removal
Material	RESIST
Time	1
Rate	1 (um/min)
VAR:Time	0

VAR:Rate	0

14.OXIDIZE step

step name (string)	Grow_Gate_Dry
Type	DRY
Time	45
Temp	1100
Ramping Rate	0
Rho-O2	1
Rho-HCl	0
VAR:Time	0
VAR:Temp	0
VAR:Rho-O2	0
VAR:Rho-HCl	0

15.INLINE step

step name (string)	IL_gate_ox
Location	<446.808502 549.436768>
Thickness	yes
Resistivity	no
Si_Junction	no
Si_SheetResistance	no

16.PHOTOLITH step

step name (string)	Photolith_Cnts
Wavelength	4358A
Type	1_to_1
Dose	150
Distance	6
Resist_Thickness	1
Time	10
Sign	POSITIVE
Mask_Name	CNT
VAR:Dose	0
VAR:Distance	0
VAR:Resist	0
VAR:Time	0

17.ETCH step

step name (string)	Define_Contacts
Material	OXIDE
Time	1
Rate	0.1 (um/min)
VAR:Time	0
VAR:Rate	0

18.ETCH step

step name (string)	Photoresist_removal
Material	RESIST
Time	1
Rate	1 (um/min)
VAR:Time	0
VAR:Rate	0

19.DEPOSIT step

step name (string)	Metallization
Material	METAL
Rate	0.3 (um/min)
Time	1
Temperature	900
VAR:Rate	0
VAR:Time	0
VAR:Temperature	0

20.INLINE step

step name (string)	IL_Al
Location	<446.808502 553.191467>
Thickness	yes
Resistivity	yes
Si_Junction	no
Si_SheetResistance	no

21.PHOTOLITH step

step name (string)	Photolith_Metal
Wavelength	4358A
Type	1_to_1
Dose	150
Distance	6
Resist_Thickness	1
Time	10
Sign	POSITIVE
Mask_Name	MTL
VAR:Dose	0
VAR:Distance	0
VAR:Resist	0
VAR:Time	0

22.ETCH step

step name (string)	Pattern_metal
Material	METAL

Time	1
Rate	0.3 (um/min)
VAR:Time	0
VAR:Rate	0

23.ETCH step

step name (string)	Photoresist_removal
Material	RESIST
Time	1
Rate	1 (um/min)
VAR:Time	0
VAR:Rate	0

24.INLINE step

step name (string)	PMOS_Final
Location	<227.784729 556.946106>
Thickness	yes
Resistivity	yes
Si_Junction	yes
Si_SheetResistance	yes

25.LOCATE_MOS_MANUAL step

step name (string)	Locate_MOS.Manual
Type	PMOS
Cutline_Start	<98.873589 554.443054>
Cutline_End	<798.498047 555.694641>
Gate	<454.317871 539.424255>
Source	<225.281586 618.272827>
Drain	<675.844727 615.769653>
Field	<439.299103 802.252808>
Source_Contact	<224.030029 554.443054>
Drain_Contact	<675.844727 550.688354>

26. MOS_PHYSICALS step

step name (string)	mos_extract

27.PHYSICALS_2_SPICE

step name (string)	calc_SPICE
Device	All_Of_Them

28.Physicals_2_NV

step name (string)	Physicals_2_NV
Device	All_Of_Them

Bibliography

1. Proceedings - International Workshop on Defect and Fault Tolerance on VLSI Systems
   title: Circuit-Level Modeling of Spot Defects
   author(s): Dinesh Gaitonde and D. M. H. Walker
   date: 1991

2. IEEE International Conference on Computer-Aided Design; Digest of Technical Papers
   title: Fast Incremental Netlist Compilation of Hierarchical Schematics
   author(s): Larry G. Jones
   date: 1989

3. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
   title: DVLASIC: Catastrophic Fault Yield Simulation in a Distributed Processing Environment
   author(s): D. M. H. Walker and Daniel S. Nydick
   date: June 1990

4. Proceedings - International Conference on Wafer Scale Integration
   title: Soft-Programmable Bypass Switch Design for Defect-Tolerant Arrays
   author(s): D. M. H. Walker
   date: 1990

5. Circuits, Systems, and Signal Processing
   title: Fault Prediction for Analog Circuits
   author(s): Ben-Lu Jiang, Chin-Long Wey, and Li-Juan Fan
   date: 1988

6. Circuits, Systems, and Signal Processing
   title: Comments on "Fault Prediction for Analog Circuits"
   author(s): V. C. Prasad and S. N. Rao Pinjala
   date: 1990

7. Circuits, Systems, and Signal Processing
title: Reply to Comments on "Fault Prediction for Analog Circuits"
author(s): Ben-Lu Jiang, Chin-Long Wey, and Li-Juan Fan
date: 1990

8. Circuits, Systems, and Signal Processing
title: Further Comments on "Fault Prediction for Analog Circuits"
author(s): V. C. Prasad and S. N. Rao Pinjala
date: 1990

9. IEEE International Symposium on Circuits and Systems
title: Built-In Self-Test (BIST) Design of Large-Scale Analog Circuit Networks
author(s): Chin-Long Wey, Ben-Lu Jiang, and Gregory M. Wierzba
date: 1989

10. International Journal of Circuit Theory and Applications
title: Fault Prediction Process for Large Analogue Circuit Networks
author(s): Ben-Lu Jiang and Chin-Long Wey
date: April 1989

11. IEEE Design and Test
title: Inductive Fault Analysis of MOS Integrated Circuits
author(s): John P. Shen, W. Maly, and F. Joel Ferguson
date: December 1985

12. IEEE Design and Test
title: PROD: A VLSI Fault Diagnosis System
author(s): Peter Odryna and Andrzej J. Strojwas
date: December 1985

13. IEEE Transactions on Circuits and Systems
title: A DC Approach for Analog Fault Dictionary Determination
author(s): Walter Hochwald and John D. Bastian
date: July 1979

14. IEEE Transactions on Computer-Aided Design
title: A Pattern Recognition Based Method for IC Failure Analysis
author(s): Andrzej J. Strojwas and Stephen W. Director
date: January 1985

15. IEEE International Test Conference
title: Systematic Characterization of Physical Defects for Fault Analysis of MOS IC Cells
author(s): W. Maly, F. J. Ferguson, and J. P. Shen
date: 1984

16. title: Computer-Aided Design Application to Fault Detection and Isolation Techniques
author(s): R. E. Tucker and L. P. McNamee
date: around 1977, exact date not available

17. IEEE Transactions on Computer-Aided Design
title: Simulation of Spatial Fault Distributions for Integrated Circuit Yield Estimations
author(s): Charles H. Stapper
date: December 1989

18. IEEE Transactions on Computer-Aided Design
title: Detection of Catastrophic Faults in Analog Integrated Circuits
author(s): Linda Milor and V. Visvanathan
date: February 1989

19. IEEE Transactions on Computer-Aided Design
title: VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits
author(s): Hank Walker and Stephen W. Director
date: October 1986

20. IEEE Transactions on Computer-Aided Design
title: VLSI Yield Prediction and Estimation: A Unified Framework
author(s): Wojciech Maly, Andrzej J. Strojwas, and Stephen W. Director
date: January 1986

21. Proceedings of the IEEE
title: Sources of Failures and Yield Improvement for VLSI and Restructurable Interconnects for RVLSI and WSI: Part I - Sources of Failures and Yield Improvement for VLSI
author: Tulin Erdim Mangir
date: June 1984

22. Proceedings of the IEEE
title: Sources of Failures and Yield Improvement for VLSI and Restructurable Interconnects for RVLSI and WSI: Part II - Restructurable Interconnects for RVLSI and WSI
author: Tulin Erdim Mangir
date: December 1984

23. IEEE ISCAS
title: A Robust Simulation-Before-Test Technique for DC Analog Fault Diagnosis
authors: V. Visvanathan, E. Szeto, and A. Tits
date: 1984

24. IEEE Transactions on Computer-Aided Design of Integrated Circuits and
Systems
title: Statistical Simulation of the IC Manufacturing Process
authors: Wojciech Maly and Andrzej J. Strojwas
date: July 1982

25. IEEE Transactions on Computer-Aided Design
title: An Extrapolated Yield Approximation Technique for Use in Yield Maximization
authors: Dale E. Hocevar, Michael R. Lightner, and Timothy N. Trick
date: October 1984

26. IEEE Transactions on Computer-Aided Design
title: Statistics Associated with Spatial Fault Simulation Used for Evaluating Integrated Circuit Yield Enhancement
author: Charles H. Stapper
date: March 1991

27. IEEE Transactions on Computer-Aided Design
title: Modeling of Lithography Related Yield Losses for CAD of VLSI Circuits
author: Wojciech Maly
date: July 1985

28. **Proceedings of the IEEE**
title: Integrated Circuit Yield Statistics
authors: Charles H. Stapper, Frederick M. Armstrong, and Kiyotaka Saji
date: April 1983

29. Solid State Electronics
title: Some Consideration in the Formulation of IC Yield Statistics
author: S. M. Hu
date: 1979

30. IEEE Transactions on Computer-Aided Design
title: Fabrics II: A Statistically Based IC Fabrication Process Simulator
authors: Sani R. Nassif, Andrzej J. Strojwas, and Stephen W. Director
date: January 1984

31. IEEE Transactions on Computer-Aided Design
title: Realistic Yield Simulation for VLSIC Structural Failures
authors: Ihao Chen and Andrzej J. Strojwas
date: November 1987

32. Evaluation Engineering
title: What Can Happen to an IC In Your System?
author: Howard K. Dicken
date: November/December 1978

33. IEE Colloquium
title: Modelling for Intelligent Fault Diagnosis - Integrating Numerical and Qualitative Techniques
authors: R. Corea, M. T. Tham, and A. J. Morris
date: February 26, 1992

34. IEE Colloquium
title: Fault Diagnosis in Analogue Electronics Without Fault Models or Prior Experience
authors: A. J. Wakeling and A. McKeon
date: February 26, 1992

35. IEEE Systems Readiness Technology Conference, AUTOTESTCON 90
title: An Automatic Diagnosis System with Fuzzy Diagnostic Approach for Linear Analog Circuits
authors: Deng Guang-Hua and Tang Ren-Heng
date: 1990

36. IEEE Design and Test of Computers
title: Fault Diagnosis in Analog Circuits Using Element Modulation
authors: Alvernon Walker, Winser E. Alexander, and Parag K. Lala
date: March 1992

37. IEEE Design and Test of Computers
title: Analog Circuit Fault Diagnosis; Based on Sensitivity Computation and Functional Testing
authors: Mustapha Slamani and Bozena Kaminska
date: March 1992

38. IEEE International Test Conference Proceedings
title: Extraction and Simulation of Realistic CMOS Faults using Inductive Fault Analysis
authors: F. Joel Ferguson and John P. Shen
date: 1988

39. IEEE International Test Conference Proceedings
title: Testing for Parametric Faults in Static CMOS Circuits
authors: F. Joel Ferguson, Martin Taylor, and Tracy Larrabee
date: 1990

40. IEEE International Test Conference Proceedings
title: Test Pattern Generation for Realistic Bridge Faults in CMOS ICs
authors: F. Joel Ferguson and Tracy Larrabee
date: 1991

41. IEEE Transactions on Computer-Aided Design
title: Detection of Multiple Faults in MOS Circuits
author: F. Joel Ferguson
date: September 1990

42. IEEE International Test Conference Proceedings
title: Yield Diagnosis Through Interpretation of Tester Data
authors: Wojciech Maly, Bonnie Trifilo, and Randall A. Hughes
date: 1987

43. IEEE Transactions on Computer-Aided Design
title: SIMPL-2: (SIMulated Profiles from the Layout - Version 2)
authors: Keunmyung Lee and Andrew R. Neureuther
date: February 1988

44. IEEE International Test Conference Proceedings
title: RYE: A Realistic Yield Simulator for VLSIC Structural Failures
authors: Ihao Chen and Andrzej J. Strojwas
date: 1987

45. IEEE Journal of Solid-State Circuits
title: The Process Engineer's Workbench
authors: Andrzej J. Strojwas and Stephen W. Director
date: April 1988

46. CMU Publication
title: VLASIC System User Manual Release 1.3
author: Duncan Moore Henry Walker
date: August 3, 1990

47. 28th ACM/IEEE Design Automation Conference Proceedings
title: A Semiconductor Wafer Representation Database and its Use in the PREDITOR Process Editor and Statistical Simulator
authors: D.M.H. Walker, C.S. Kellen, and A.J. Strojwas
date: 1991

48. CMU Publication
title: The PREDITCR Process Editor and Statistical Simulator
authors: D.M.H. Walker, C.S. Kellen, and A.J. Strojwas
date: March 1991

49. IEEE Transactions on Computer-Aided Design of Integrated Circuits and
Systems
title: Fault Detection and Classification in Linear Integrated Circuits: An Application of Discrimination Analysis and Hypothesis Testing
authors: Benjamin R. Epstein, Martin Czigler, and Steven R. Miller
date: January 1993

50. IEEE International Test Conference Proceedings
title: Fault Modeling for the Testing of Mixed Integrated Circuits
authors: Anne Meixner and Wojciech Maly
date: 1991

51. PREDITOR User's Manual Version 2.0
author: Chris Kellen
date: April 9, 1992

MISSION

OF

ROME LABORATORY

Mission. The mission of Rome Laboratory is to advance the science and technologies of command, control, communications and intelligence and to transition them into systems to meet customer needs. To achieve this, Rome Lab:

a. Conducts vigorous research, development and test programs in all applicable technologies;

b. Transitions technology to current and future systems to improve operational capability, readiness, and supportability;

c. Provides a full range of technical support to Air Force Materiel Command product centers and other Air Force organizations;

d. Promotes transfer of technology to the private sector;

e. Maintains leading edge technological expertise in the areas of surveillance, communications, command and control, intelligence, reliability science, electro-magnetic technology, photonics, signal processing, and computational science.

The thrust areas of technical competence include: Surveillance, Communications, Command and Control, Intelligence, Signal Processing, Computer Science and Technology, Electromagnetic Technology, Photonics and Reliability Sciences.